Scientific requirements and dimensioning for the MICADO-MAORY SCAO RTC

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on behalf of the MICACO & MAORY team

Global overview of the instrument

- Shown mounted under MAORY.

Design spaces:

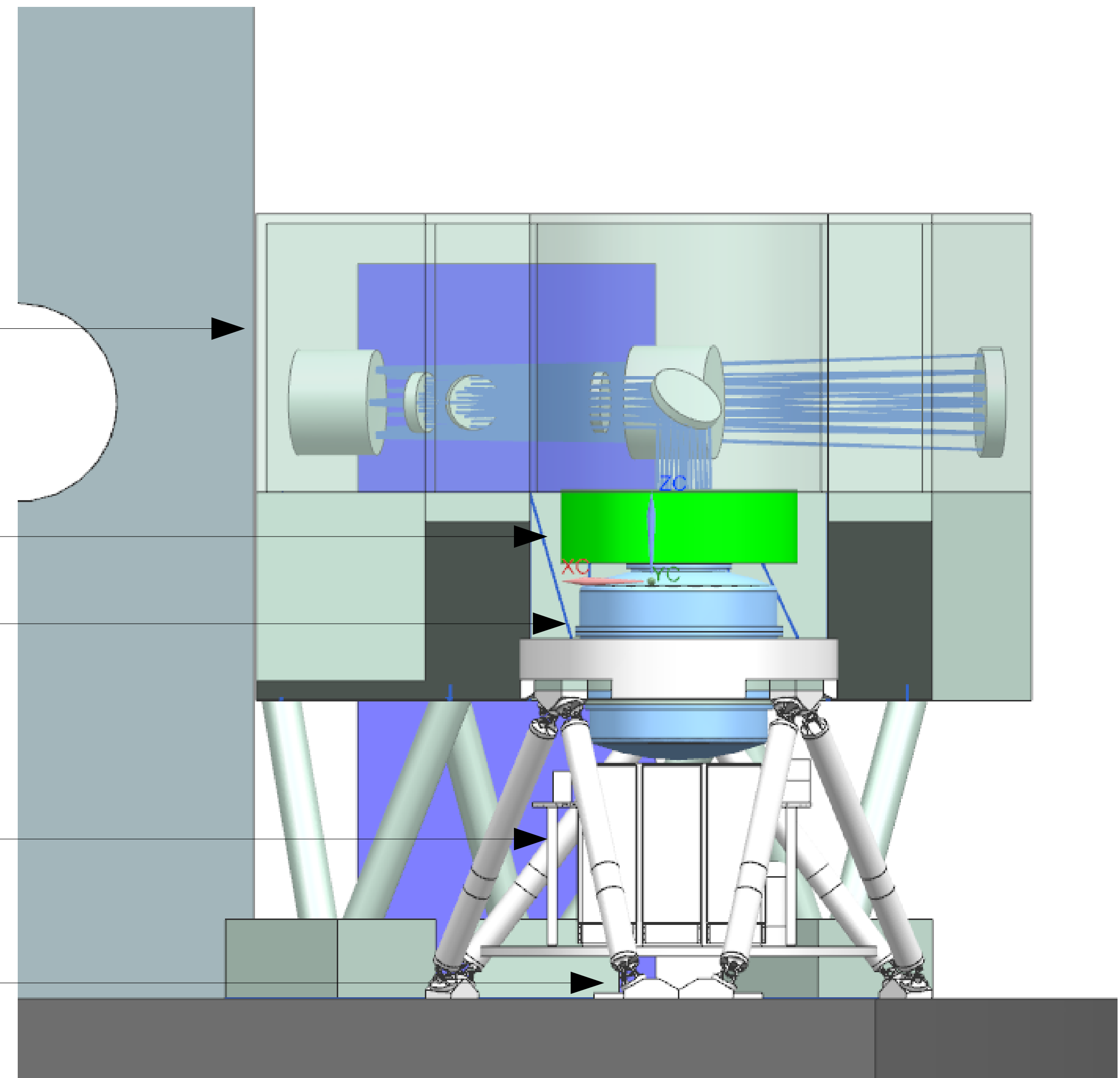
MAORY & MICADO calibration unit

SCAO WFS + MAORY NGS-WFS (Green Doughnut)

Cryostat & derotator

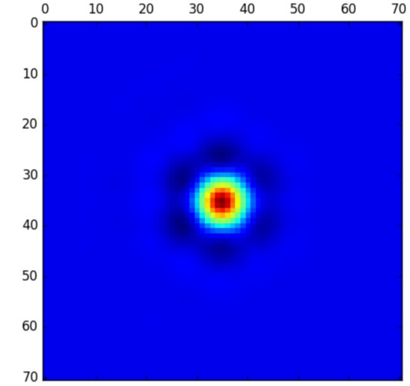
Electronics (co-rotating)

Cable-wrap

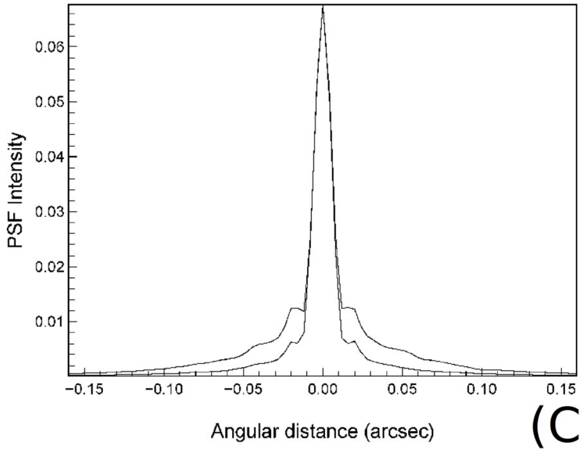


SCAO performance

- Based on end-to-end GPU simulations (Seen in Florian FERREIRA & Sebastien DURAND)
  - Maximum strehl ~60% with SH WFS
    - Limited by M4 and telescope WFE budget
    - Residual tip-tilt ~3mas

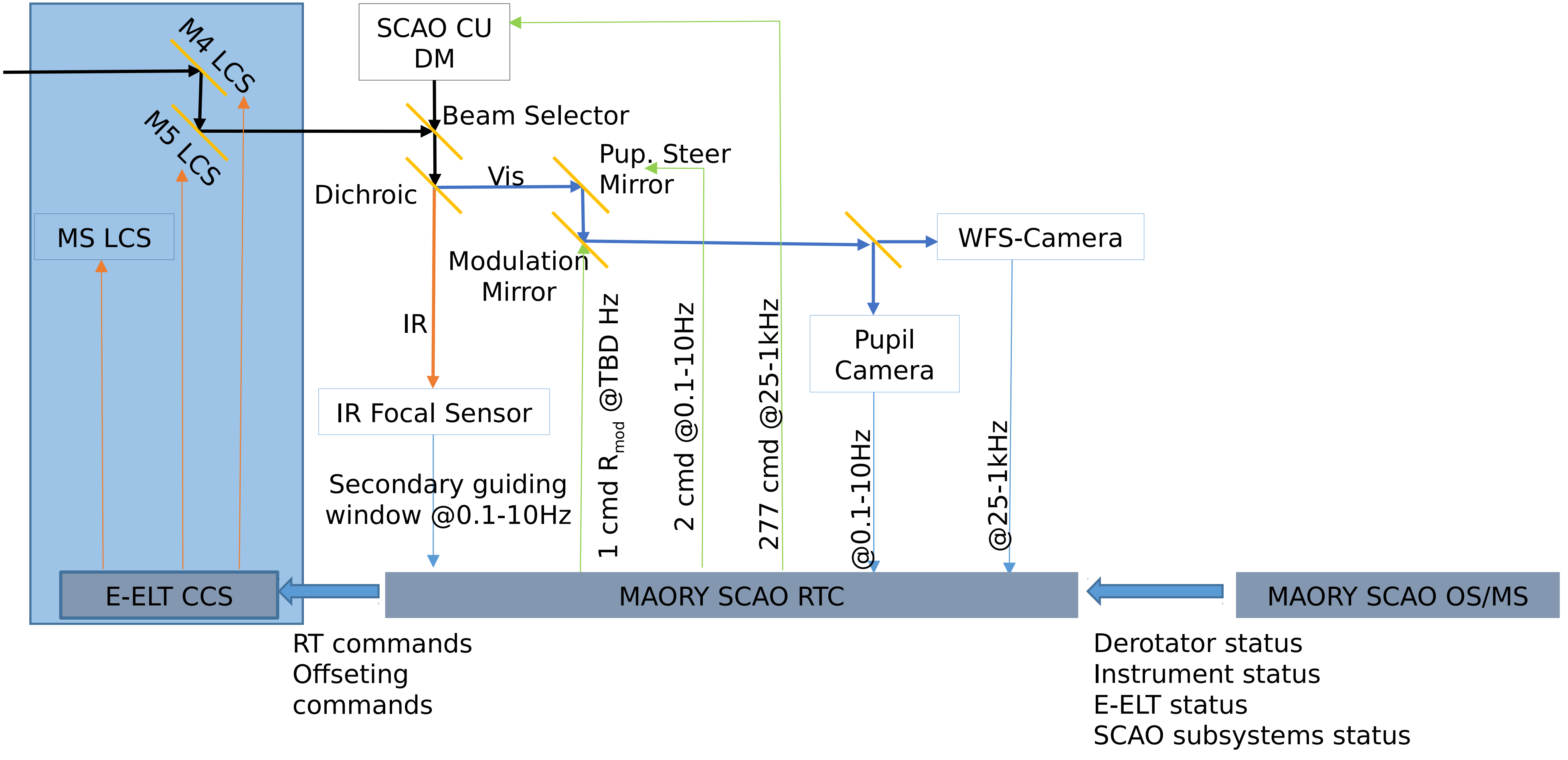


- Based on analytic formula
  - Anisoplanatism
    - Different to 8-m telescopes, because E-ELT diameter is comparable to L0.
    - Although strehl ratio is low, PSF retains a diffraction limited core even far off-axis
  - PSF with radial & transverse cuts, 30” off-axis, for realistic L0 profile (K-band Strehl ~6%)



(CLÉNET+ 13, 14)

MICADO-MAORY SCAO subsystem mode overview



MICADO-MAORY SCAO in few numbers

- WFS data transfer dimensionning
  - 1 Pyramid WFS 240x240 pixels @1kHz ~1Gb/s
  - 1 SH WFS 880x840 pixels @1kHz ~11.8Gb/s

	Baseline	***Backup***
Type	Pyramid WFS	Shack-Hartmann WFS
Number	1	1
Wavelength	0.45 µm – 0.9 µm (TBC)	0.45 µm – 0.9 µm (TBC)
Geometry	80 x 80 to 100 x 100sub-aperture (TBC)	80 x 80 to 100 x 100sub-aperture (TBC)
Sub-aperture size	2 x 2 pixel	4x4 or 6x6 (TBC)
No. of used sub-apertures	TBD	TBD
Detector type	CCD220	NGSD
Detector size	240 x 240	880 x 840
Used frame size	TBD	800 x 800
Frame rate	25 Hz-1 kHz	25 Hz-1 kHz
Readout modes	Frame-transfer + 8-channel readout (TBC)	Rolling shutter (TBC)

- To relax this contraint, WFS could send only slopes and intensities to the RTC

MICADO-MAORY SCAO in few numbers

- MICADO-MAORY SCAO baseline
  - Framerate: 1000Hz
  - 1 Pyramid WFS:
    - 240x240 pixels @1kHz ~1Gb/s
    - 80x80 ssp, let say ~10k measurements
  - ELT CCS: ~5k commands
  - Command matrix for a least-square controler ~1.6Gb ↔ 200MB

MICADO-MAORY SCAO RTC Performance assessment

- Hard real-time subsystem:
  - Baseline, linear control with matrix-vector multiply
  - MVM Performance: 100 Gflops (but memory-bound)
  - Determinism: 10% jitter over a 1000 FPS framerate so max peak to peak jitter of 100µs is required
- Supervision module: optimization of hard-real time parameters
  - Main powerful task: regular control matrix update
  - SVD Performance: 750Gflop (but also memory-bound)
  - Addressed with a standard HPC cluster

GPU Computing performance

- For the computation part, 1 GPU is enough :

Model	Architecture	Theoretical peak performance single precision (TFLOPS)	Memory bandwidth (Gb/s)	ECC	Energy consumption (W)
NVidia Tesla K40	Kepler	4.29	2304	Yes	235
NVidia Tesla K80	Kepler	8.5	3840	Yes	300
NVidia P100	Pascal	10.6	5856	Yes	300

- But, MVM is a io bound problem, the memory bandwidth is the first performance indicator.

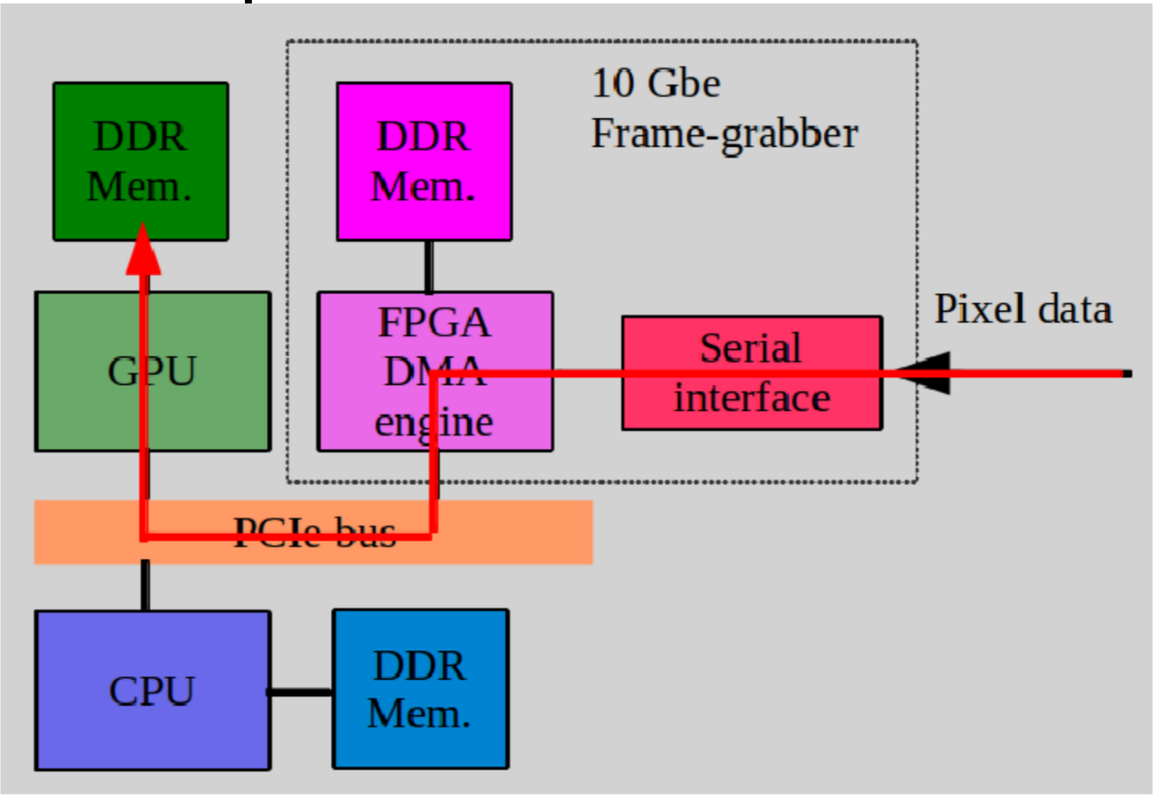
	K20C	K40	K80	P100
theo	1664	2304	1920 (x2)	5856
ECC off	1400 (84%)	1888 (82%)	1536 (x2, 80%)	3696 (63%)
ECC on	1200 (72%)	1664 (72%)	1360 (x2, 70%)	Not tested

  - NGPU = CEIL(CR(in *Gflops*) / (B(in *Tb/s*) * FPP)) = 1 GPU P100

    *100 Gflops / (3.696 Tb/s * 32) = 0.85*

GPU Computing performance

- Need for tailored data acquisition process to feed the GPU with pixel data



- See Maxime LAINE & Julien BERNARD presentations Wednesday

CPU Computing performance

- Intel Xeon CPU / Xeon Phi
  - Between 100 & 500 GB/s memory bandwidth per processing units
  - Up to 5 CPUs or 1 KNL (see David JENKINS presentation tomorrow)
- Reference solution using standard libraries and portable code
- Need vectorization on Xeon Phi to meet peak performance
- Long term availability of Xeon Phis ?

FPGA Computing performance (see Roberto BIASI presentation)

- ARRIA 10AS066 SoC
  - 1.5GHz ARM dual-core Cortex-A9 co-processor
  - 1855 DSP blocks
  - 5.2MB int. RAM
  - max. 48 XCVR links
- ARRIA 10AX115
  - 1518 DSP blocks
  - 6.6MB int. RAM
  - max. 96 XCVR
- high cost of dedicated IP development, but deterministic by design and robust solution

TBU: To be updated

ESO specific constraints

- ESO is gathering instrument specifications to build a standardized AO RTC approach
- ESO will define a RTC toolkit for instrument consortia
- ESO will publish a call for tenders on commun RTC prototyping for all instrusments (mid 2017)
- Need to take into account E-ELT specificities : e.g. M4 control, handover between telescope control system and AO system …
- Instrument calibration issues : limited daytime slots for instrument calibration may impose efficient strategies with strong computing constraints

Conclusions

- MICADO Preliminary Design Phase in progress
(PDR planned in 10/2018, PDR MAORY in 02/2018)
- Concerns about the ESO development plan schedule vs. MICADO & MAORY PDR
- LESIA is leading the RTC for the MICADO-MAORY SCAO mode
- LESIA is proposing to build this RTC but concerns (in terms of resources) if ESO RTC standards are in the end orthogonal to the outcome of the GF project (see Damien Gratadour presentation)
- Interaction with ESO: needed to be compliant with RTC toolkit and design full RTC pipeline including M4 control / interaction with telescope