Green Flash

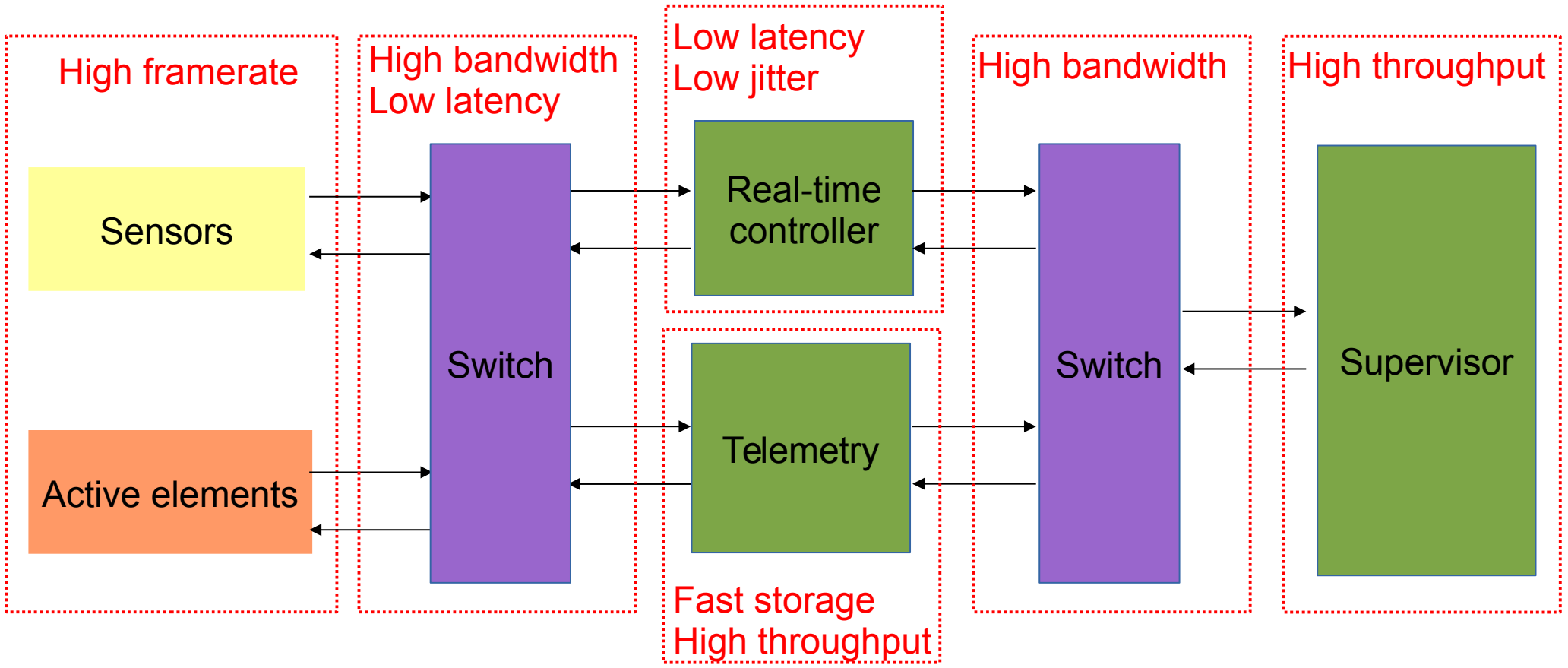
High performance computing for real-time science

Building a smart interconnect strategy

AO4RTC4 workshop, Paris 2016

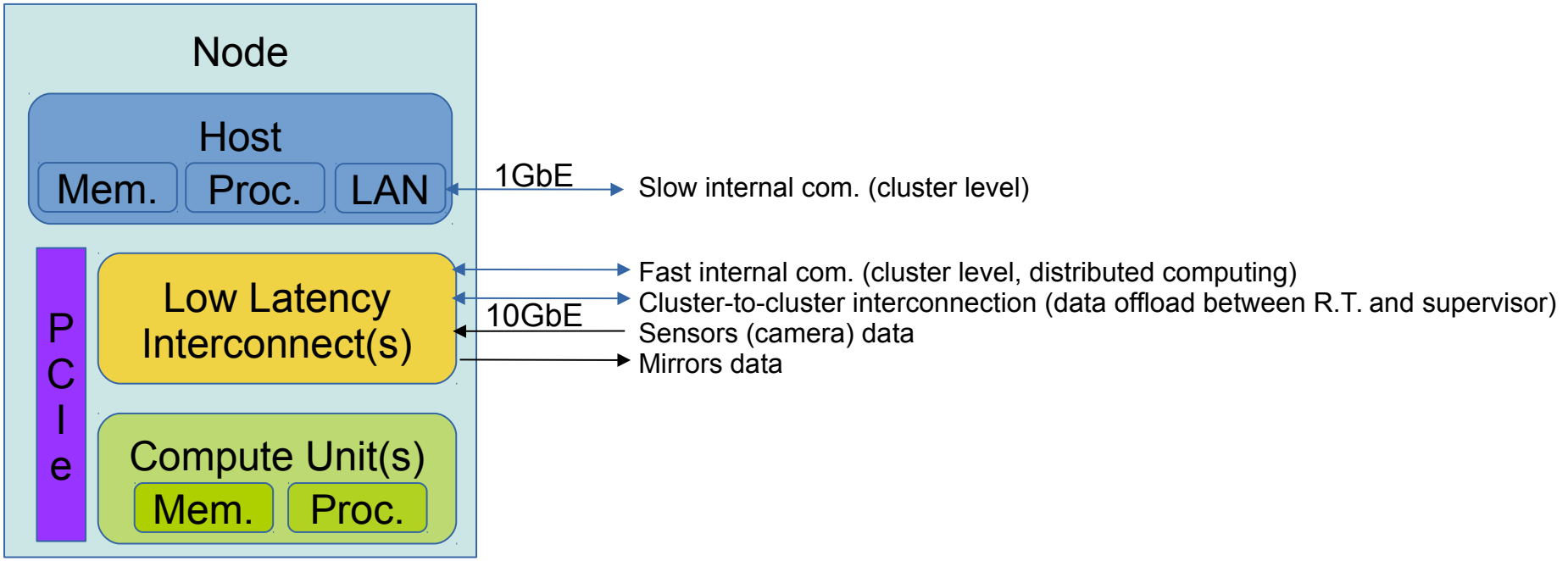
Project #671662 funded by European Commission under program H2020-EU.1.2.2 coordinated in H2020-FETHPC-2014

AO RTC concept

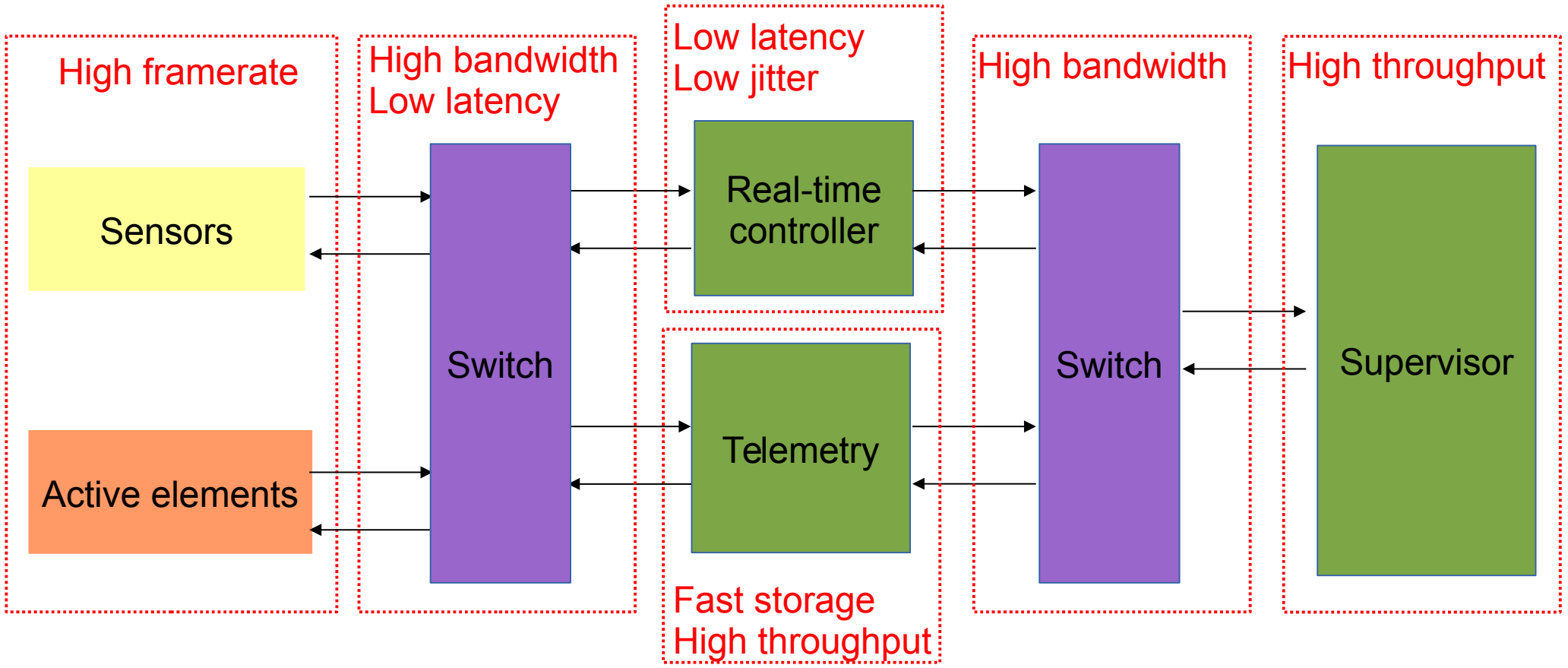


AO RTC concept

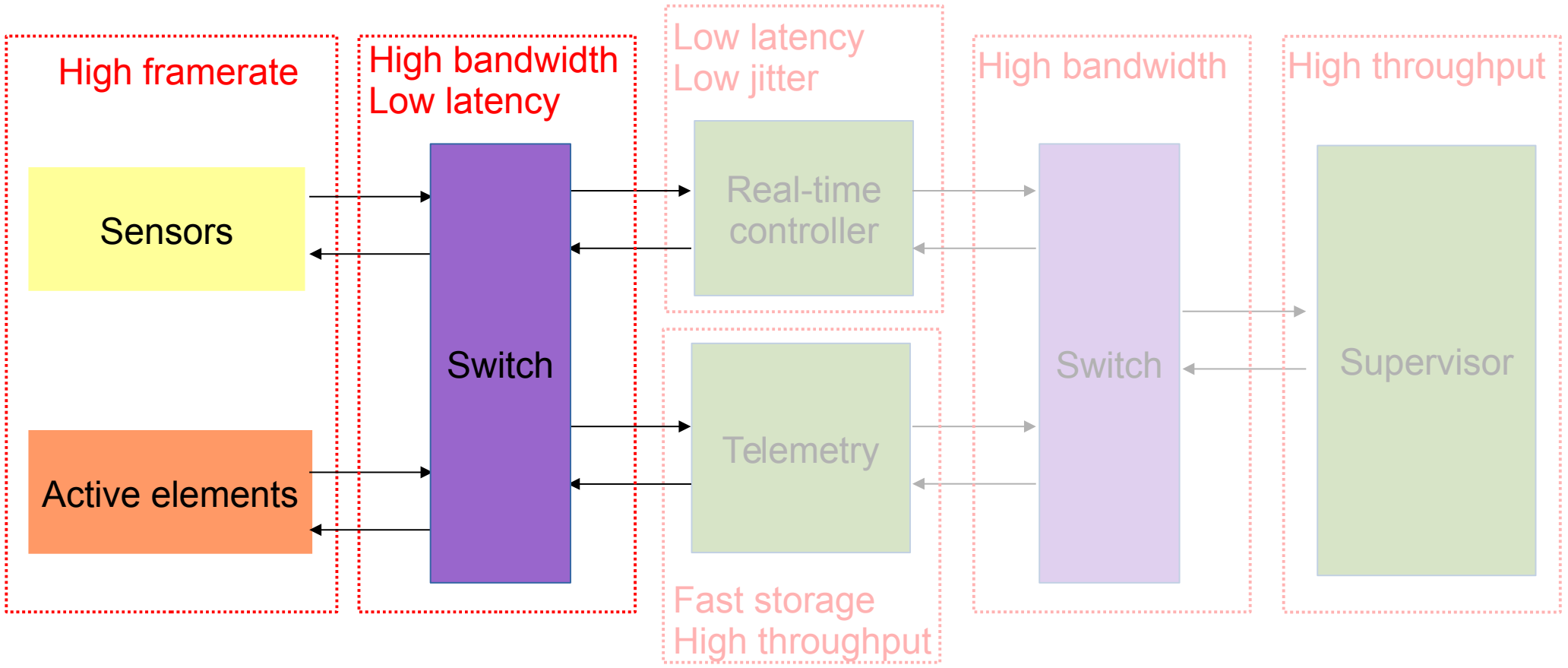
- Single generic node concept



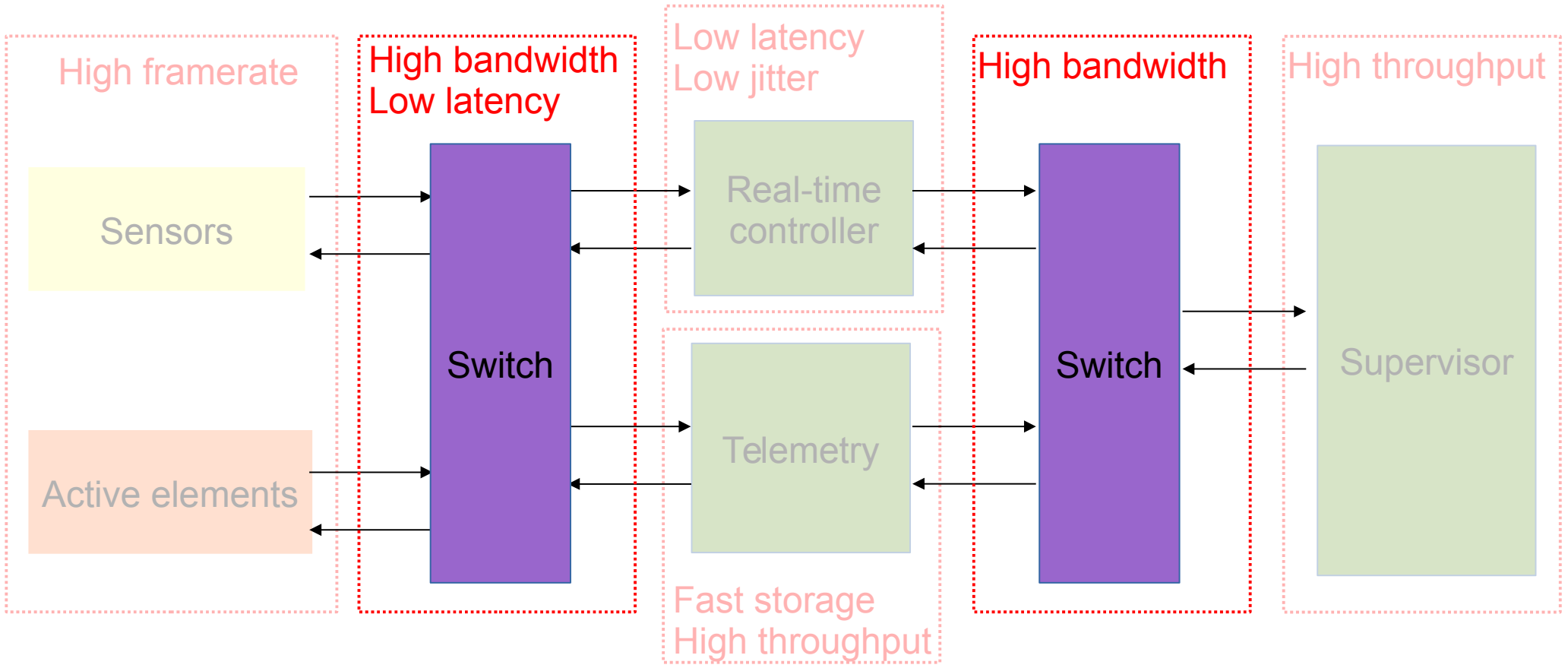
AO RTC concept



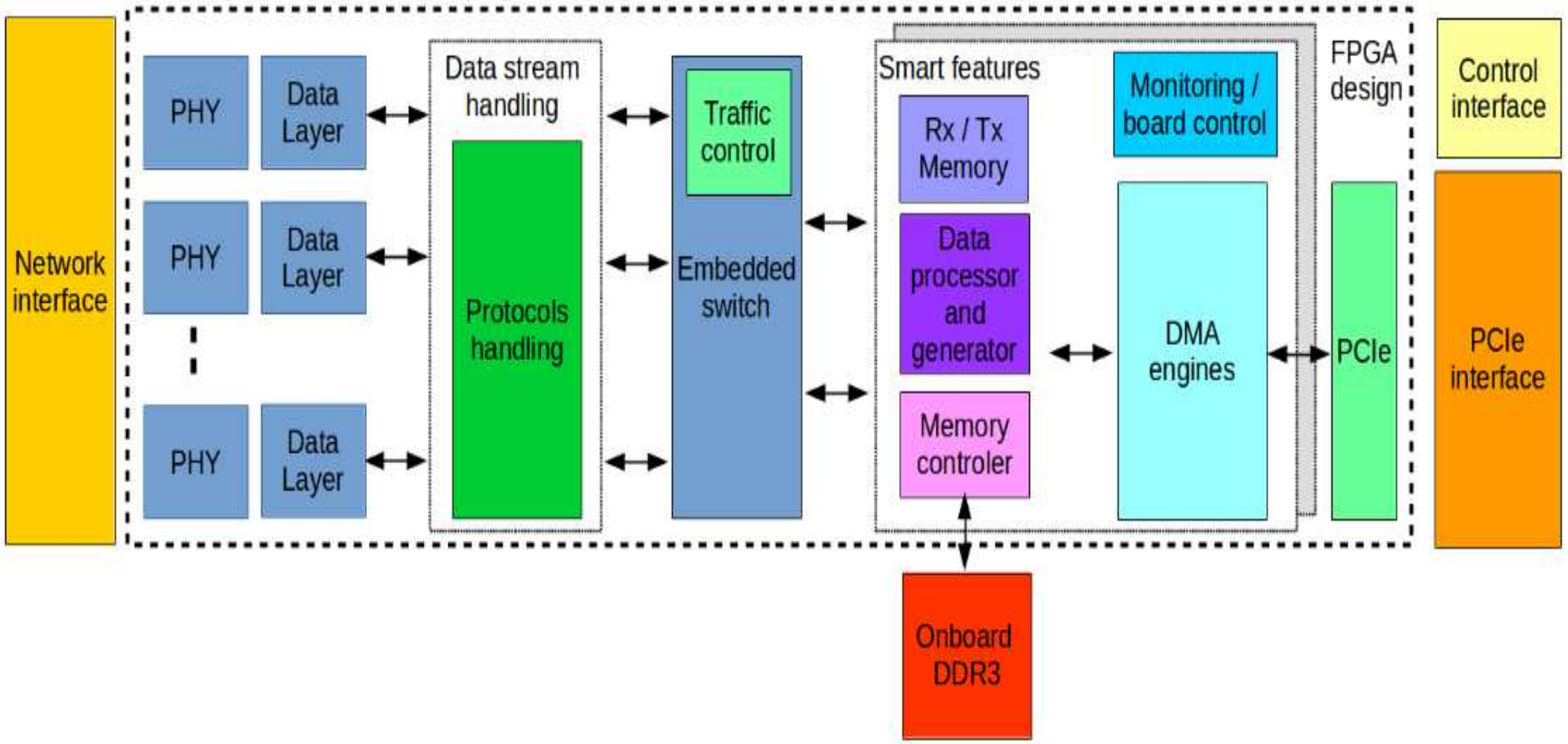
AO RTC concept : data streams



AO RTC concept : local / global interco.



Smart interconnect architecture

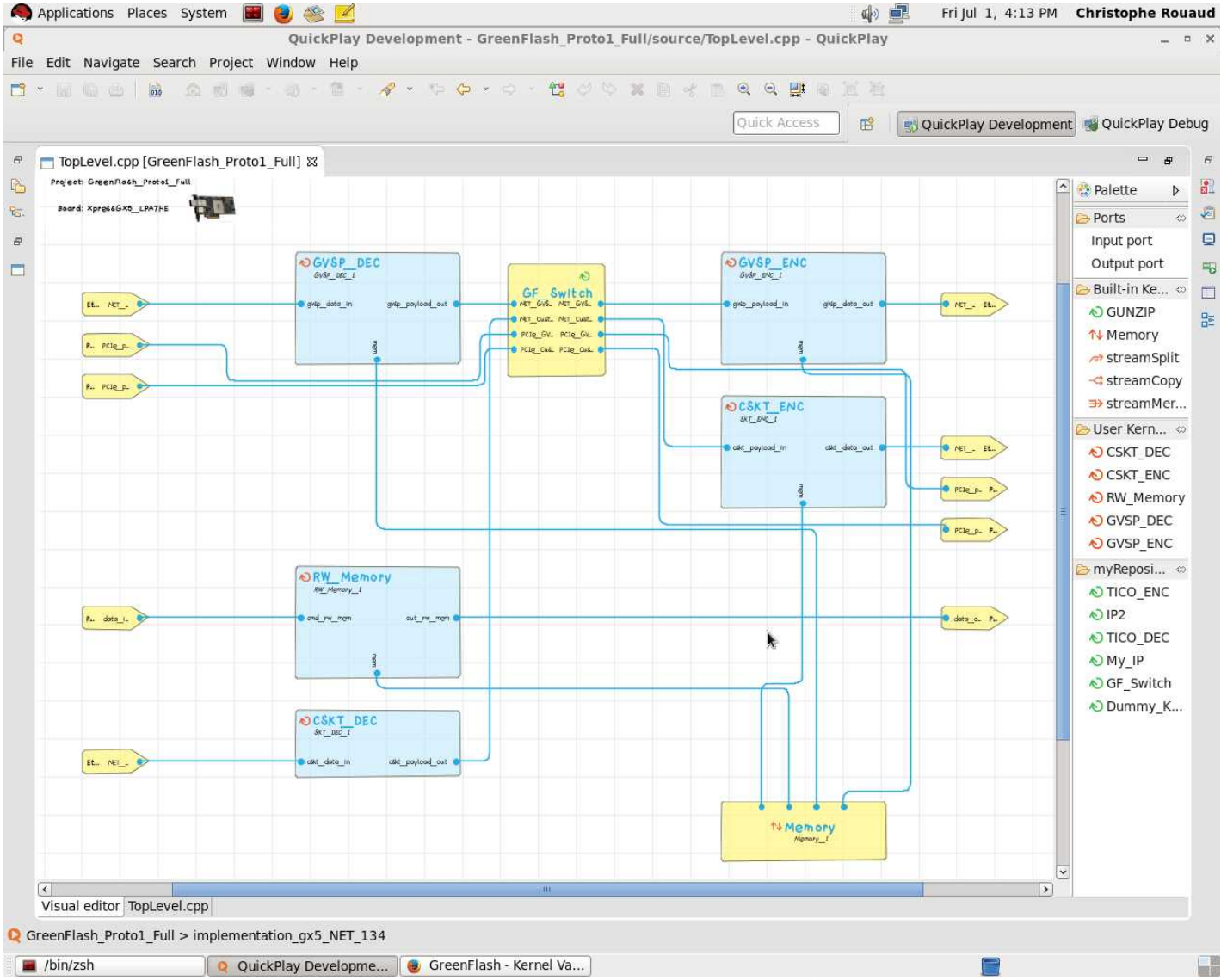


Smart interconnect concept

- Eased devel. process using the QuickPlay tool from PLDA

QuickPlay™

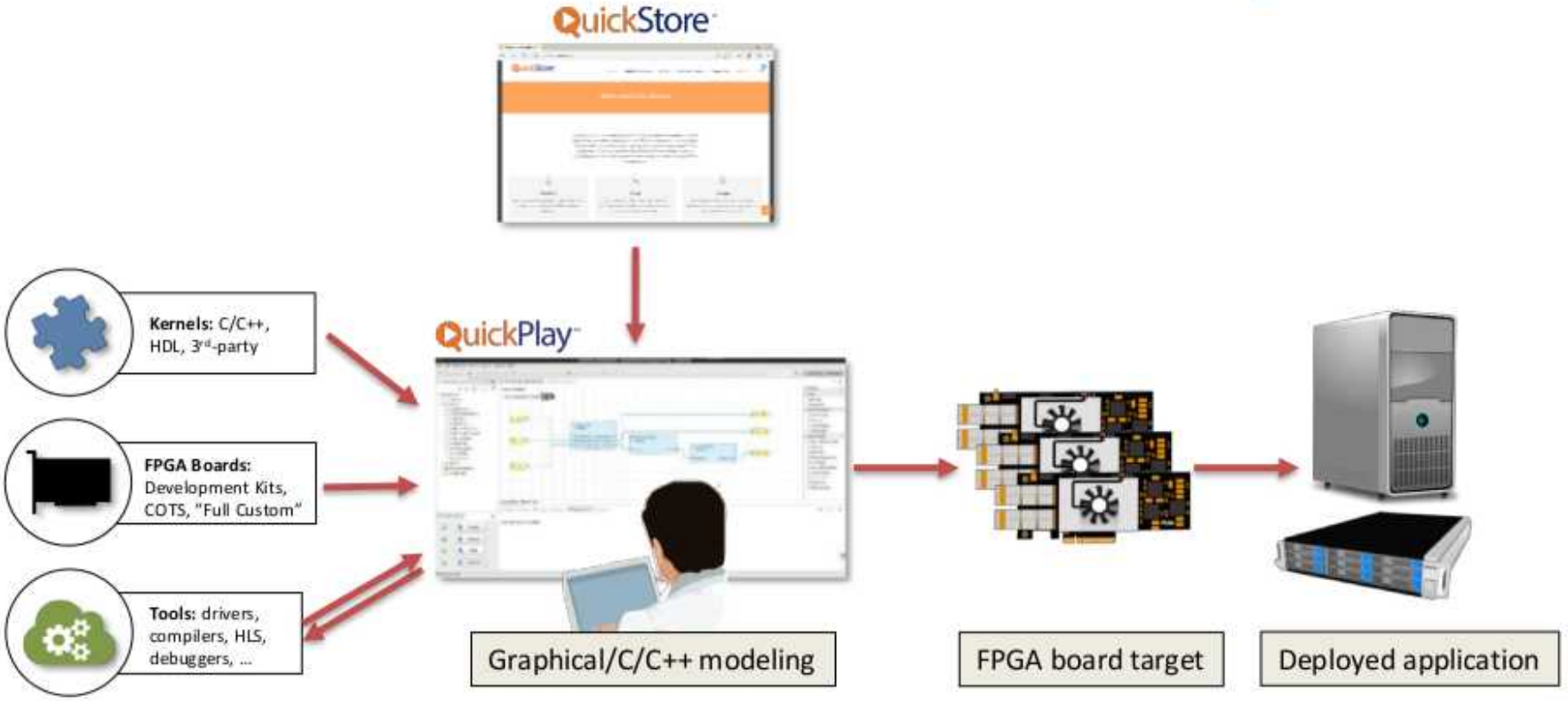
QuickStore™



QuickPlay

QuickPlay™

Introducing QuickPlay



QuickPlay

QuickPlay™

FPGA Design with QuickPlay IDE

1. **MODEL**
   - C/C++ functional modeling

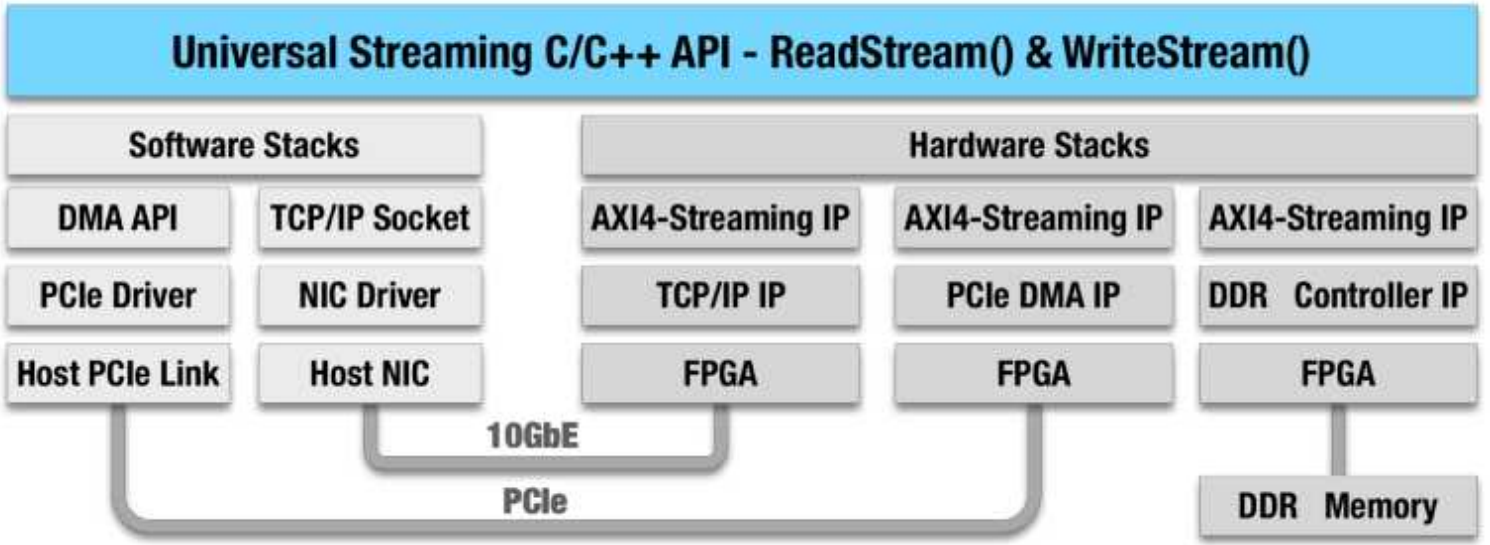
2. **VERIFY & VALIDATE**
   - Desktop execution of system functional model

3. **BUILD**
   - Hardware implementation: HLS, Logic Synthesis, P&R

4. **EXECUTE**
   - FPGA based system hardware execution

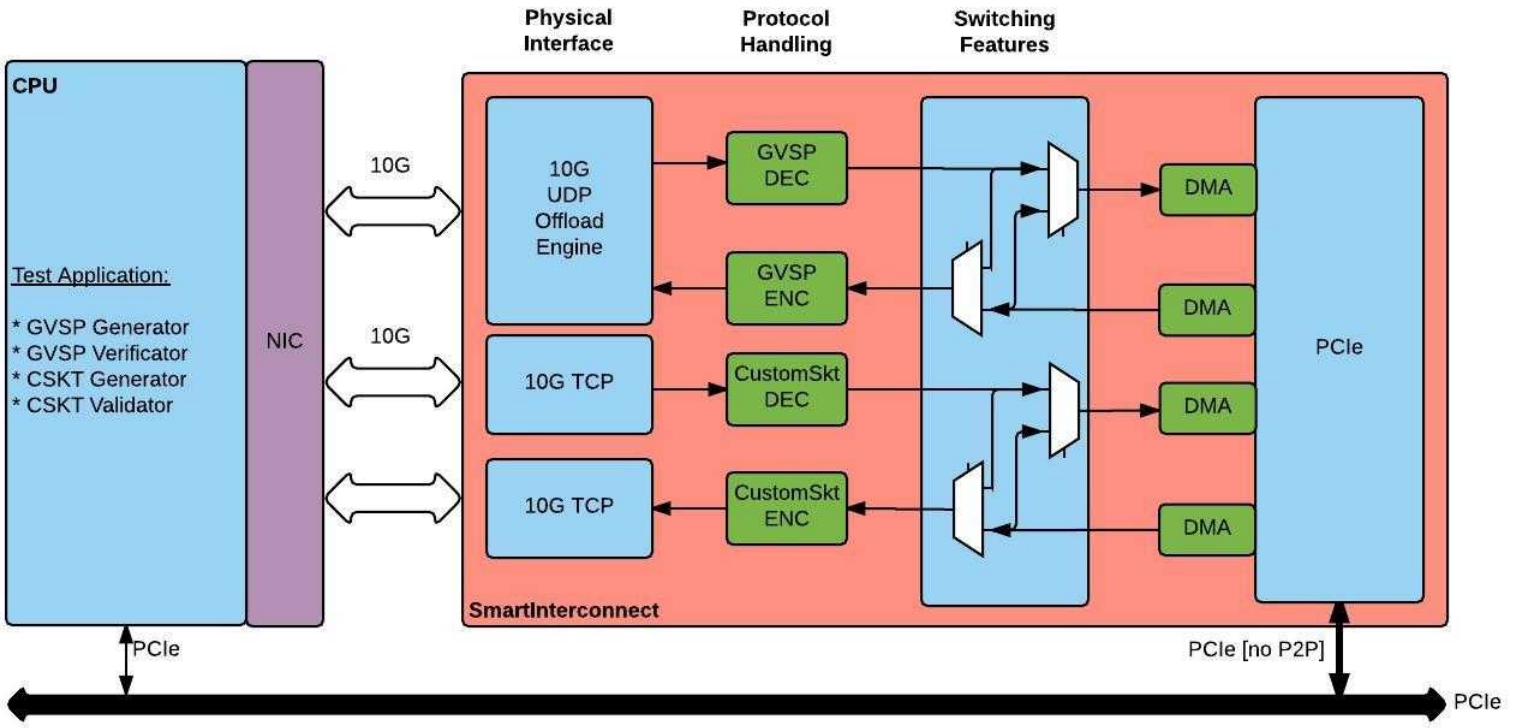
QuickPlay

QuickPlay™ Hardware Accelerator Abstraction Layer



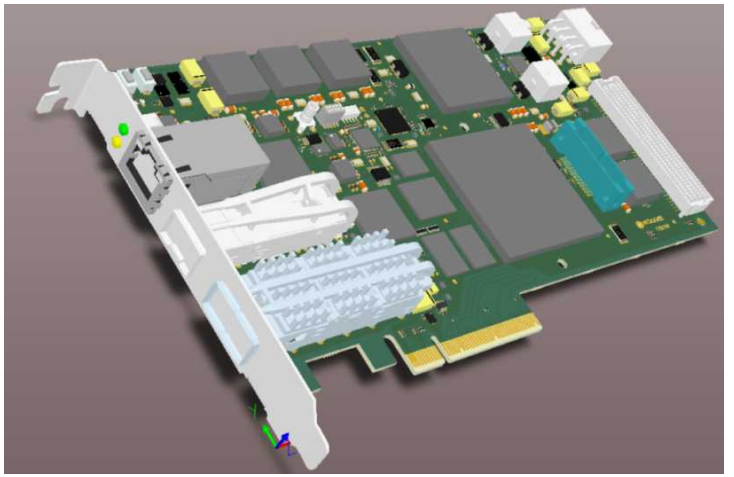
Smart interconnect concept

- Link with high level API / application



Smart interconnect prototyping

- Single generic design / multiple target boards
  - ExpressK-US board (hosting a Kintex UltraScale from Xilinx)
  - ExpressGX V board (hosting a Stratix V from Altera)
  - µXlink board from microgate (hosting a Arria 10 board from Altera)



MICROGATE

Faster Technology

LESIA

Laboratoire d'Études Spatiales et d'Instrumentation en Astrophysique

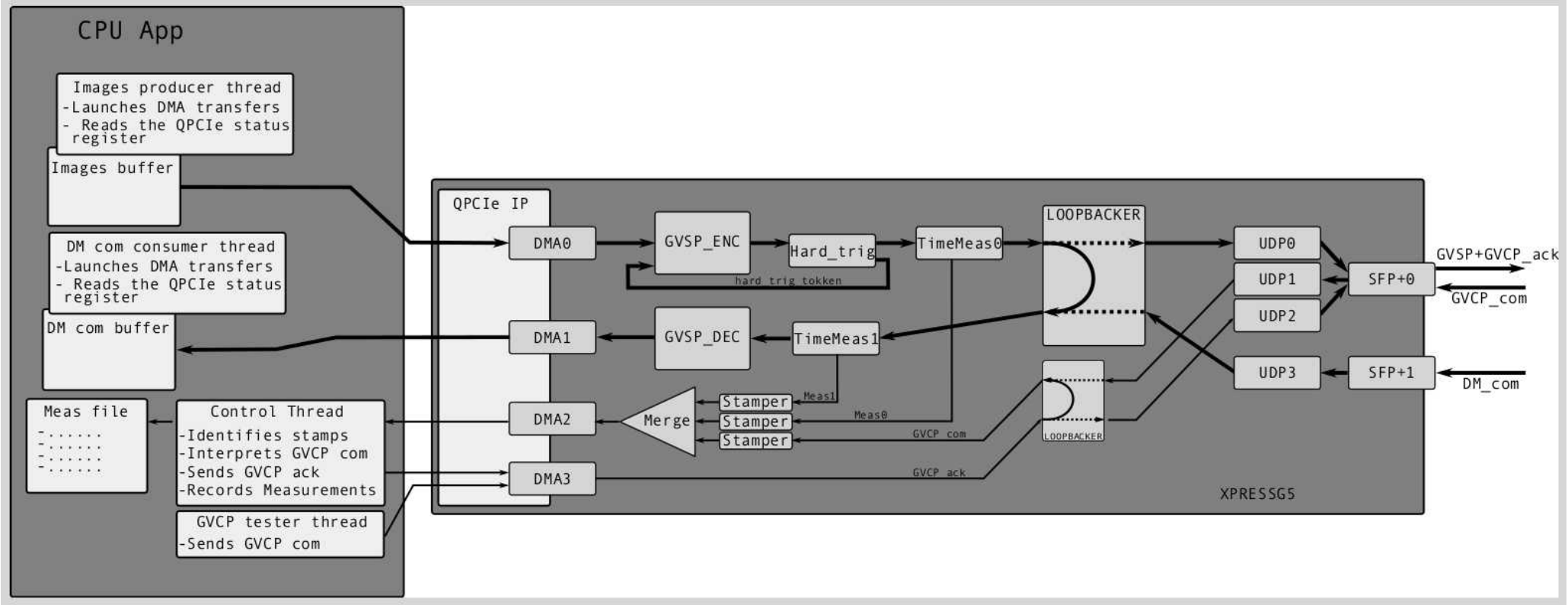
Durham University

MICROGATE

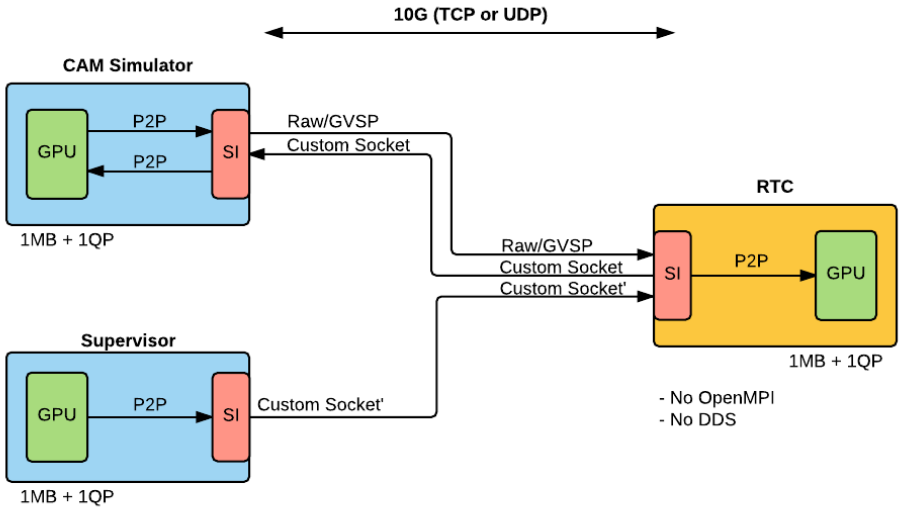
PLDA

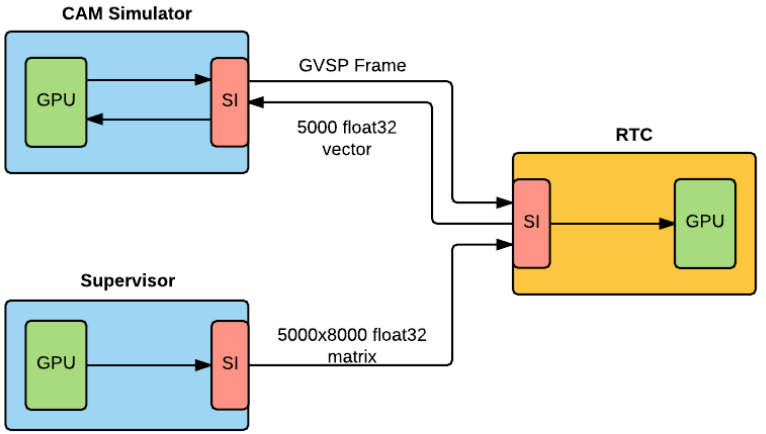
Smart interconnect concept

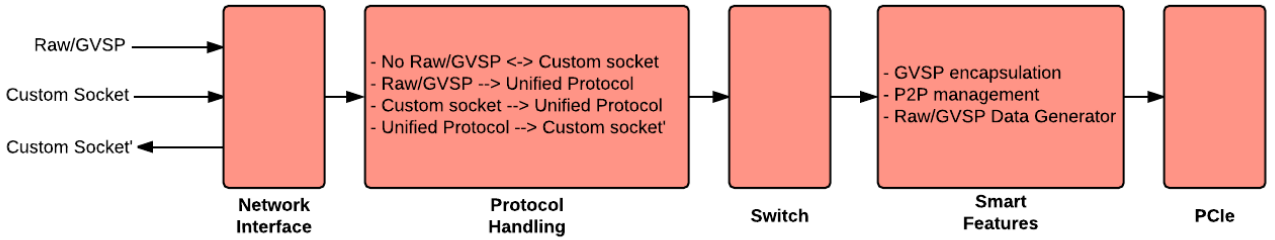
- Fake camera / fake DMC concept developed at LESIA



Smart interconnect prototyping







Summary

Smart interconnect concept

- Cope with heterogeneous data streams in the system
- Unified interconnect strategy
- Reduce development cost (simplified development environment) and maximize maintainability over the long term (multiple target boards)

QuickPlay tool from PLDA

- Eased FPGA development cycle
- Mix communication protocols and data processing into the same streams
- Expandable ecosystem, with QuickStore / QuickAliance

Prototyping in the lab

- SCAO ready prototype being integrated
- Single design / multiple board concept being assessed
- MCAO ready prototype will include inra-cluster communication