Green Flash
High performance computing for real-time science

A status update … (a.k.a. teaser slides)

AO4RTC4 workshop, Paris 2016
AO RTC concept

High framerate
Sensors

High bandwidth
Low latency
Low jitter
Real-time controller

Low latency
High throughput
Telemetry

High bandwidth
Switch

High throughput
Switch

High throughput
Supervisor

Active elements

Fast storage
High throughput
Introduction to Green Flash

- Program objectives: 3 research axes
  - 2 technological developments and 1 validation study
- Real-time HPC using accelerators and smart interconnects
  - Assess the determinism of accelerators performance
  - Develop a smart interconnect strategy to cope for strong data transfer bandwidth constraints
- Energy efficient platform based on FPGA for HPC
  - Prototype a main board, based on FPGA SoC and PCIe Gen3
  - Cluster such boards and assess performance in terms of energy efficiency and determinism
- AO RTC prototyping and performance assessment
  - Assemble a full functionality prototype for a scalable AO RTC targeting the MAORY system
  - Compare off-the-shelf solutions based on accelerators and new FPGA-based concept
What this is about … really

• Find the best trade-off for ELT sized AO systems RTC
  – Comprehensive assessment of existing technologies
  – Development of new custom solutions for comparison
  – Propose new development processes to reduce cost and increase maintainability

• Build a full featured RTC prototype at the largest scale possible
  – Technology down-selection from a number of criteria: performance, cost, compliance to standards, obsolescence, maintainability
  – State of the art system to be assessed in the lab, with a simulator
Project timeline

- Good convergence with H2020 ETP4HPC / E-ELT project timeline
AO RTC concept

- High framerate
- Sensors
- High bandwidth
- Low latency
- Low jitter
- Active elements
- Real-time controller
- Fast storage
- High throughput
- Telemetry
- High bandwidth
- Switch
- Supervisor
AO RTC concept: RT simulator

- High framerate
- High bandwidth
- Low latency
- Low jitter
- High throughput

Components:
- Sensors
- Active elements
- Real-time controller
- Telemetry
- Fast storage
- Switch
- Supervisor
Real-time simulator

- Emulation interface to RTCS

- Concept developed @ Durham, see Andrew Reeves presentation
Real-time simulator

- Several simulation tools:
  - Low level functional test with slow python-based simulation (SOAPy)
  - High-level tests with fast end-to-end simulation (COMPASS)
  - Performance / determinism assessment with HW pixel generator
Real-time simulator

• Using COMPASS for E2E should provide a scalable solution over the long term
  – Execution times from F. Ferreira
AO RTC concept

High framerate

Sensors

High bandwidth
Low latency

Active elements

Low latency
Low jitter

Real-time controller

Fast storage
High throughput

Telemetry

Switch

High bandwidth

Switch

High throughput

Supervisor
AO RTC concept: data pipeline

- High framerate
- Sensors
- Active elements
- High bandwidth
- Low latency
- Real-time controller
- Telemetry
- Fast storage
- High throughput
- Supervisor
RT data pipeline with accelerators

- Study the achievable perf. on GPUs

<table>
<thead>
<tr>
<th>Ctrl</th>
<th>Clock</th>
<th>Average</th>
<th>Min</th>
<th>Max</th>
<th>Jitter</th>
<th>Computation rate</th>
<th>Memory transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTC 1 device</td>
<td>device</td>
<td>0.51 ms</td>
<td>0.5 ms</td>
<td>0.52 ms</td>
<td>23 us</td>
<td>2e+02 GFlops</td>
<td>3.9e+02 GB</td>
</tr>
<tr>
<td>RTC 2 device</td>
<td>device</td>
<td>0.32 ms</td>
<td>0.31 ms</td>
<td>0.33 ms</td>
<td>12 us</td>
<td>3.1e+02 GFlops</td>
<td>6.3e+02 GB</td>
</tr>
</tbody>
</table>
RT data pipeline with accelerators

- Prototype using latest generation GPU cluster

- Concept studied at LESIA, see talks by Julien Bernard & Maxime Lainé

19/12/2016
RT data pipeline with accelerators

- Intel Xeon Phi
- First results on Knights Corner (10k meas. vector)

<table>
<thead>
<tr>
<th></th>
<th>Knights Corner</th>
<th>Knights Landing predicted</th>
<th>Knights Landing preliminary measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>MVM computation time</td>
<td>1.2-1.3 ms</td>
<td>0.9 ms</td>
<td>0.76 ms (0.63μs when optimised for thread count)</td>
</tr>
<tr>
<td>Memory bandwidth</td>
<td>165 GB/s</td>
<td>250 GB/s</td>
<td>258 GB/s TRIAD, 235 GB/s MVM</td>
</tr>
</tbody>
</table>

- Concept studied at Durham, see talk by David Jenkins
RT data pipeline with new FPGA microserver

- Exploring new concepts for HPC
RT data pipeline with new FPGA microserver

- 2 boards concepts: standard (accelerator) / standalone (w/ SOC: microserver)
RT data pipeline with new FPGA microserver

- Boards are becoming real @ Microgate!
AO RTC concept

- High framerate
- Sensors
- Active elements

- High bandwidth
- Low latency
- Low jitter
- Switch
- Telemetry
- Fast storage
- High throughput

- Real-time controller
- Switch
- Supervisor

- Low latency
- Low jitter
- High bandwidth

19/12/2016
AO RTC concept: smart interconnect

- High framerate
- Sensors
- Active elements
- High bandwidth
- Low latency
- Low jitter
- Real-time controller
- Telemetry
- Fast storage
- High throughput
- Switch
- Switch
- Supervisor
Smart interconnect concept

- Collaboration between PLDA and LESIA
- Proof of concept on a SCAO ready prototype
Smart interconnect architecture
Smart interconnect concept

- Eased devel. process using the QuickPlay tool from PLDA
AO RTC concept

High framerate - Sensors

High bandwidth - Active elements

Low latency - Switch

Low jitter - Real-time controller

High throughput - Telemetry

Fast storage - Switch

High bandwidth - Supervisor

19/12/2016
AO RTC concept: supervisor

- High framerate
- Sensors
- Low latency
- Active elements
- High bandwidth
- Low jitter
- Real-time controller
- Fast storage
- High throughput
- Telemetry
- Switch
- Supervisor
- High bandwidth
- Low latency
- Low jitter
- High throughput
Supervision for tomographic AO

- New, optimized supervision pipeline
- See talk by Nicolas Doucet
- Collaboration LESIA + KAUST (KSA)
AO RTC concept

- High framerate
- Sensors
- Active elements

- High bandwidth
- Low latency
- Low jitter
- Real-time controller
- Telemetry
- Fast storage
- High throughput

- High bandwidth
- Switch

- High throughput
- Supervisor
AO RTC concept: SW & MW

- High framerate
- Sensors
- Active elements
- High bandwidth
- Low latency
- Low jitter
- Switch
- Real-time controller
- Telemetry
- Fast storage
- High throughput
- Supervisor
- High bandwidth
SW / MW stack

- Under development in Paris & Durham
- Run a standard HPC ecosystem on the prototype boards and clusters
- Performance assessed w/r AO application (mainly linear algebra)
## Middleware options

<table>
<thead>
<tr>
<th>Role</th>
<th>Option 1</th>
<th>Option 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Pipeline</td>
<td>Zero-MQ</td>
<td>MPI</td>
</tr>
<tr>
<td>Command/Control</td>
<td>Zero-MQ</td>
<td>ICE</td>
</tr>
<tr>
<td>Telemetry</td>
<td>DDS</td>
<td>ICE</td>
</tr>
</tbody>
</table>

- Under study in Durham
- See Eddy Younger talk on Wednesday
Summary

Project on track

- PDR occurred in Jan. 2016 with feedback from community
- Prototyping activities have started with preliminary results (see per WP presentation)
- Prototyping mid-term review scheduled on Feb. 1rst 2017

Collaborations initiated

- Good feedback from the community on different aspects (HPC + instrumentation)
- Evaluate the convergence and minimize additional effort

More work needed on dissemination

- Populating public website
- Contributions to international conference and publications

Already enhancing the readiness level of commercial solutions

- Contribution to QuickPlay development
- Design of an innovative FPGA board (see Roberto’s presentation)