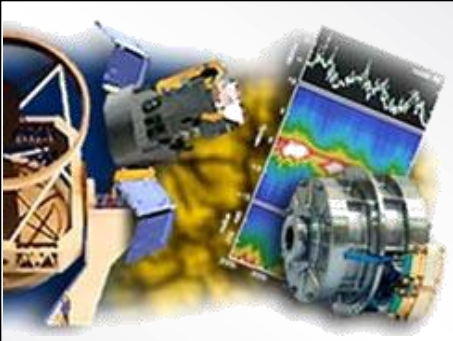
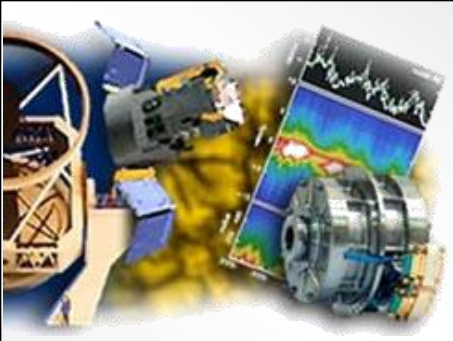


INSTITUTO DE ASTROFÍSICA DE CANARIAS

Real-time control with FPGA, GPU and CPU at IAC

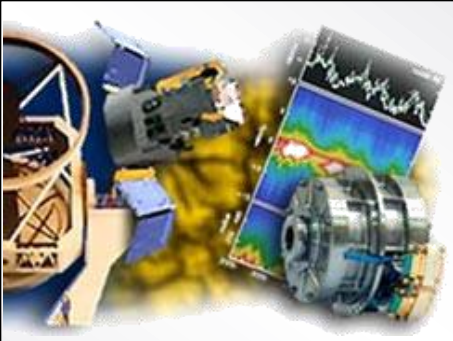
Paris, 2016-01-26

Luis Fernando Rodríguez Ramos
Instituto de Astrofísica de Canarias



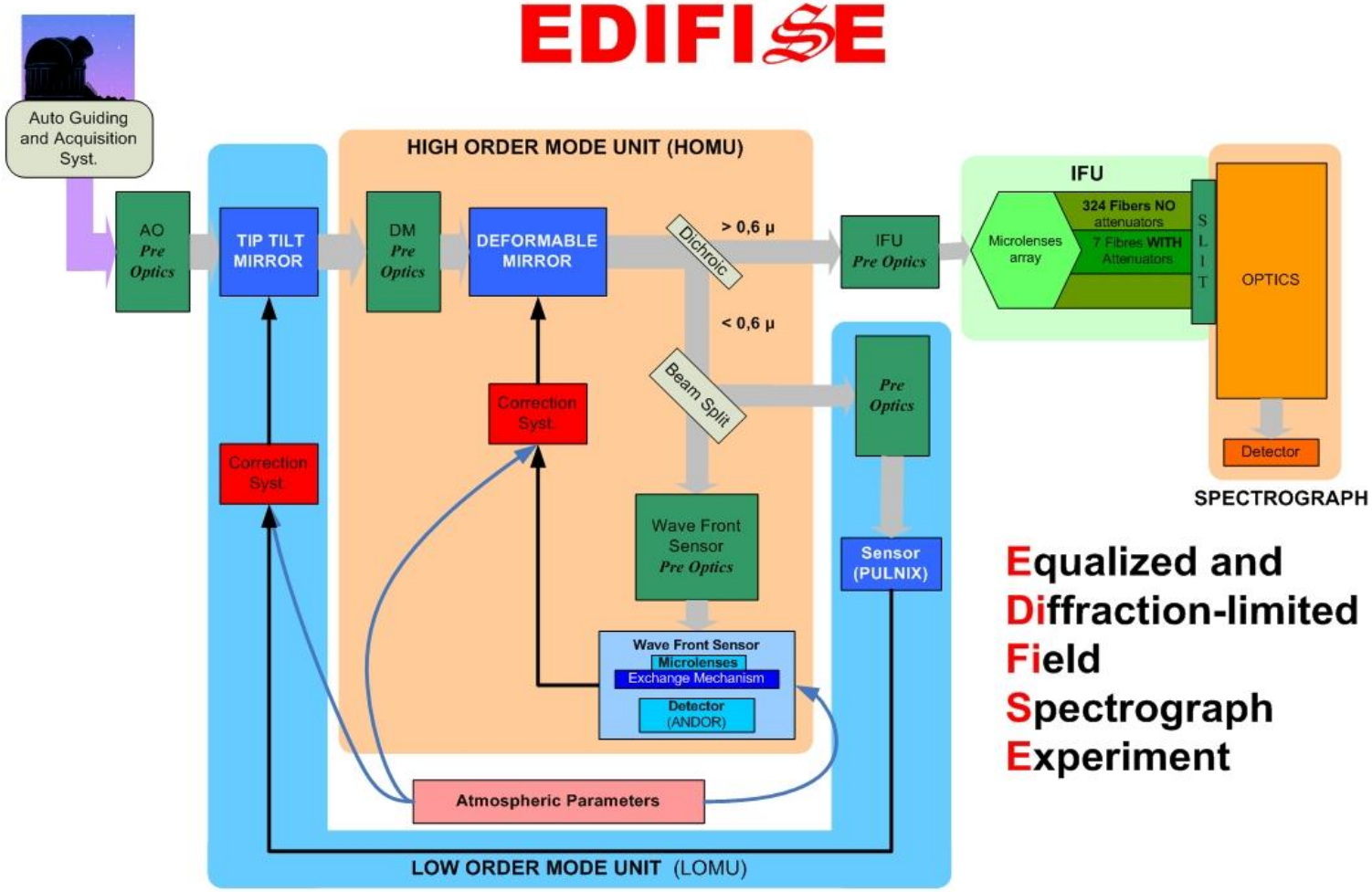
Contents

- Introduction
- Brief review of ongoing IAC Adaptive Optics projects
- Summary of control technologies used
- Technologies comparison
- Conclusions

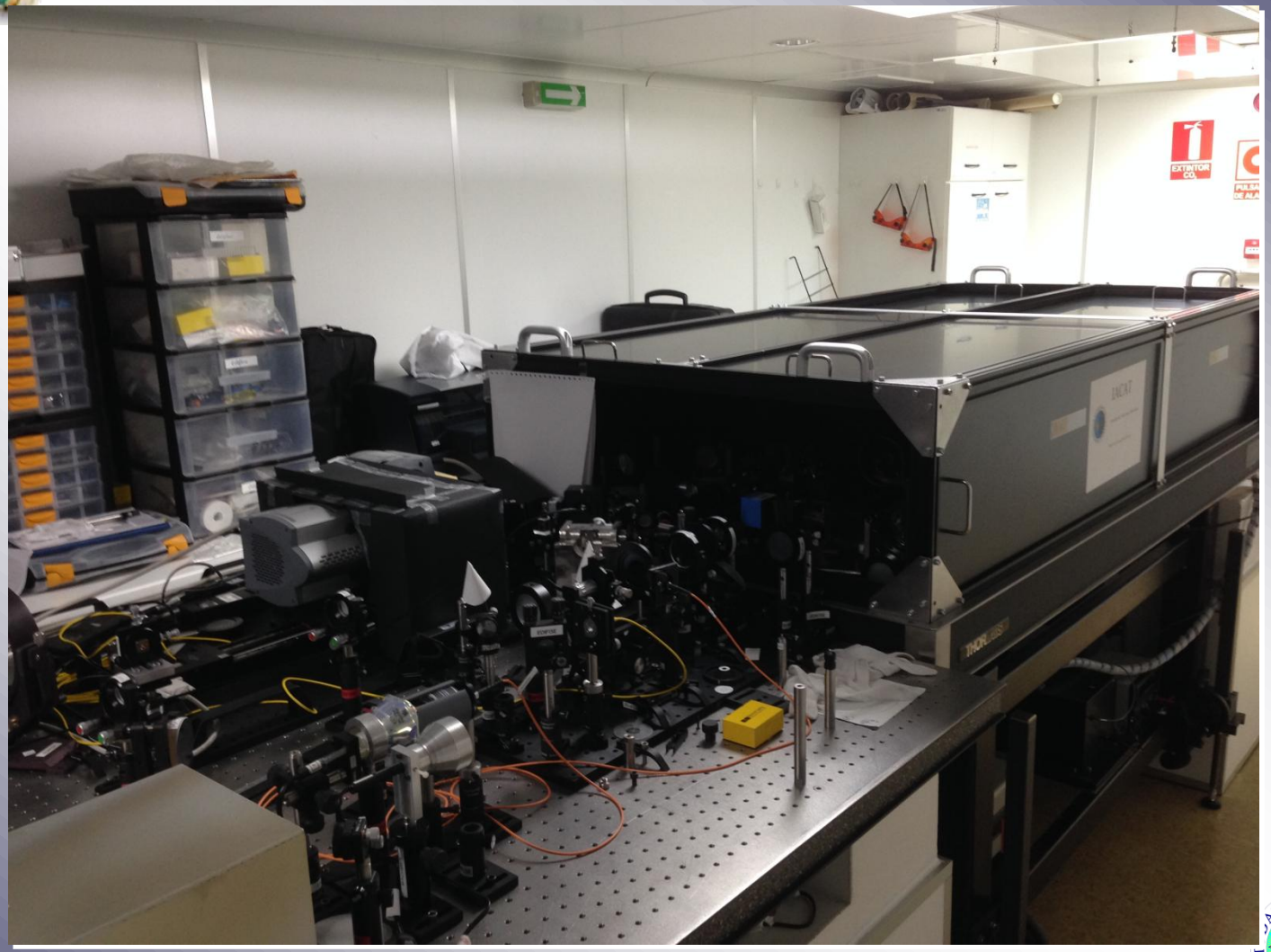


Contents

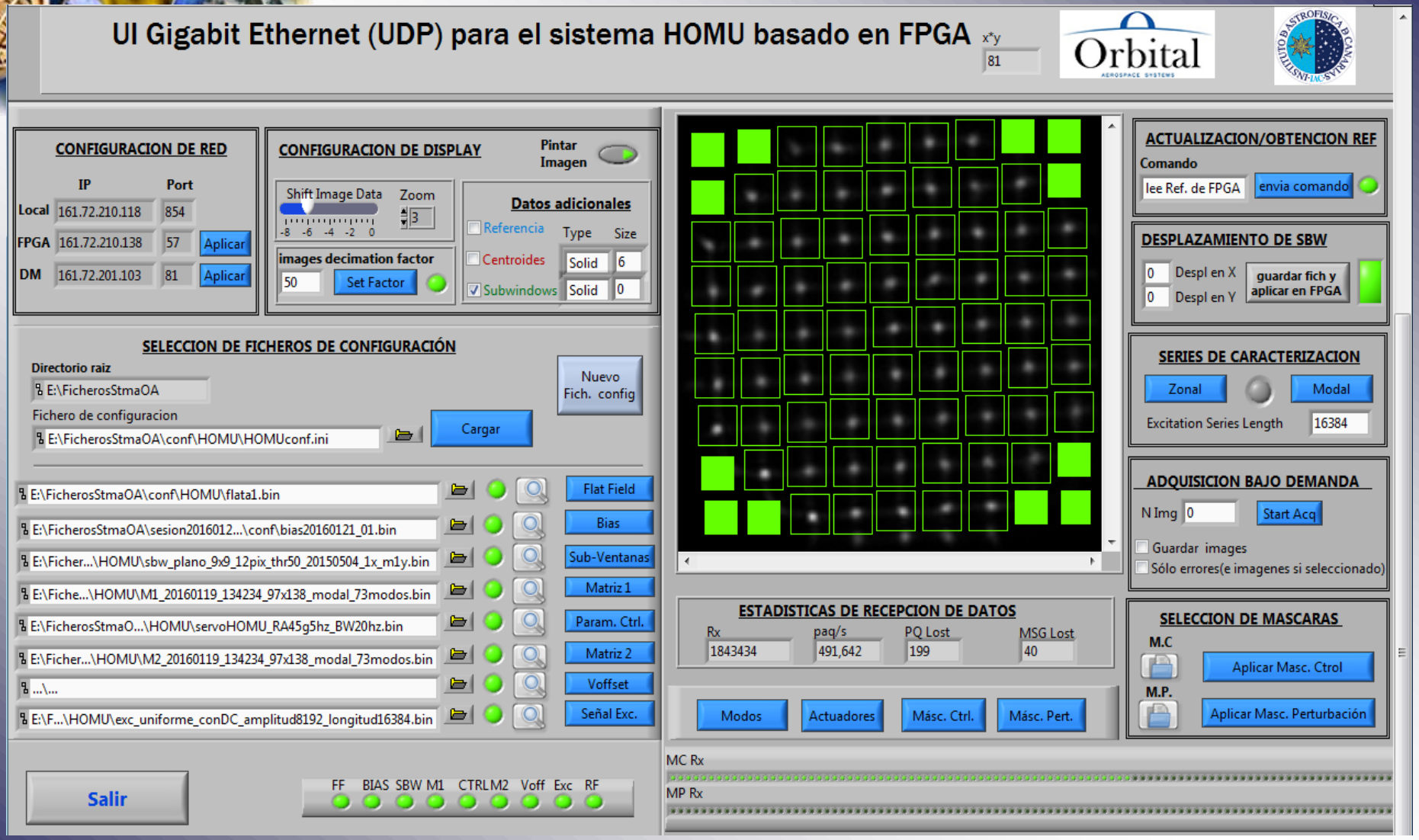
EDiFiSE

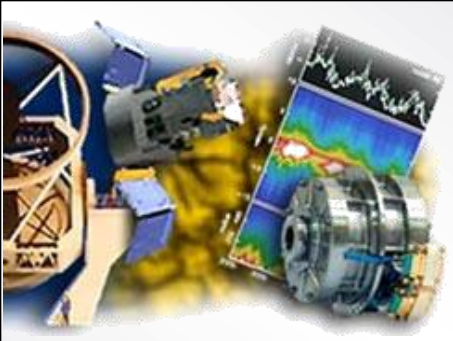

EDIFISE
Auto Guiding and Acquisition Syst.
AO Pre Optics
TIP TILT MIRROR
HIGH ORDER MODE UNIT (HOMU)
DM Pre Optics
DEFORMABLE MIRROR
Dichroic
> 0,6 μ
< 0,6 μ
Beam Split
IFU Pre Optics
IFU
Microlenses array
324 Fibers NO attenuators
7 Fibres WITH Attenuators
SLIT
OPTICS
Detector
SPECTROGRAPH
Correction Syst.
Correction Syst.
Pre Optics
Wave Front Sensor Pre Optics
Sensor (PULNIX)
Wave Front Sensor
Microlenses
Exchange Mechanism
Detector (ANDOR)
Atmospheric Parameters
LOW ORDER MODE UNIT (LOMU)
Equalized and
Diffraction-limited
Field
Spectrograph
Experiment

EDiFiSE Laboratory setup

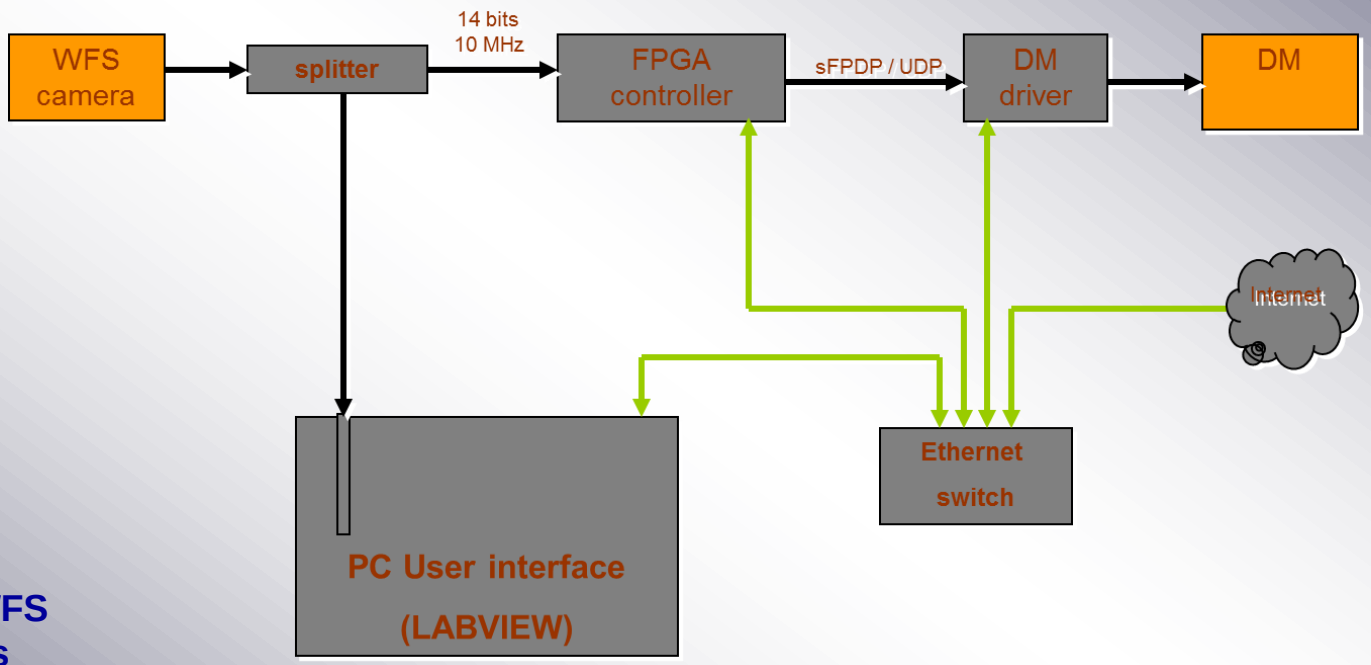


EDiFiSE GUI

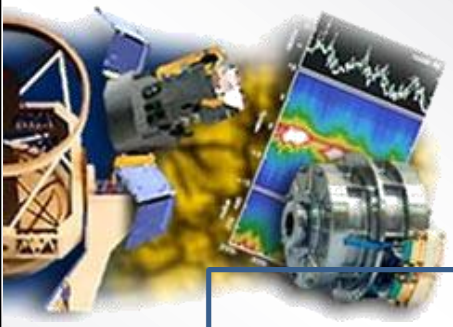

UI Gigabit Ethernet (UDP) para el sistema HOMU basado en FPGA
x*y
81
Orbital
CONFIGURACION DE RED
IP
Port
Local
161.72.210.118
854
FPGA
161.72.210.138
57
Aplicar
DM
161.72.201.103
81
Aplicar
CONFIGURACION DE DISPLAY
Pintar Imagen
Shift Image Data
Zoom
3
images decimation factor
50
Set Factor
Datos adicionales
Referencia
Type
Size
Centroides
Solid
6
Subwindows
Solid
0
SELECCION DE FICHEROS DE CONFIGURACIÓN
Directorio raiz
E:\FicherosStmaOA
Nuevo Fich. config
Fichero de configuracion
E:\FicherosStmaOA\conf\HOMU\HOMUconf.ini
Cargar
E:\FicherosStmaOA\conf\HOMU\flata1.bin
Flat Field
E:\FicherosStmaOA\sesion2016012...\conf\bias20160121_01.bin
Bias
E:\Ficher...\HOMU\sbw_plano_9x9_12pix_thr50_20150504_1x_m1y.bin
Sub-Ventanas
E:\Fiche...\HOMU\M1_20160119_134234_97x138_modal_73modos.bin
Matriz 1
E:\FicherosStmaO...\HOMU\servoHOMU_RA45g5hz_BW20hz.bin
Param. Ctrl.
E:\Ficher...\HOMU\M2_20160119_134234_97x138_modal_73modos.bin
Matriz 2
...\...
Voffset
E:\F...\HOMU\exc_uniforme_conDC_amplitud8192_longitud16384.bin
Señal Exc.
Salir
FF BIAS SBW M1 CTRL M2 Voff Exc RF
ACTUALIZACION/OBTENCION REF
Comando
lee Ref. de FPGA
envia comando
DESPLAZAMIENTO DE SBW
0
Despl en X
0
Despl en Y
guardar fich y aplicar en FPGA
SERIES DE CARACTERIZACION
Zonal
Modal
Excitation Series Length
16384
ADQUISICION BAJO DEMANDA
N Img
0
Start Acq
Guardar images
Sólo errores(e imagenes si seleccionado)
ESTADISTICAS DE RECEPCION DE DATOS
Rx
1843434
paq/s
491,642
PQ Lost
199
MSG Lost
40
SELECCION DE MASCARAS
M.C
Aplicar Masc. Ctrol
M.P.
Aplicar Masc. Perturbación
Modos
Actuadores
Másc. Ctrl.
Másc. Pert.
MC Rx
MP Rx



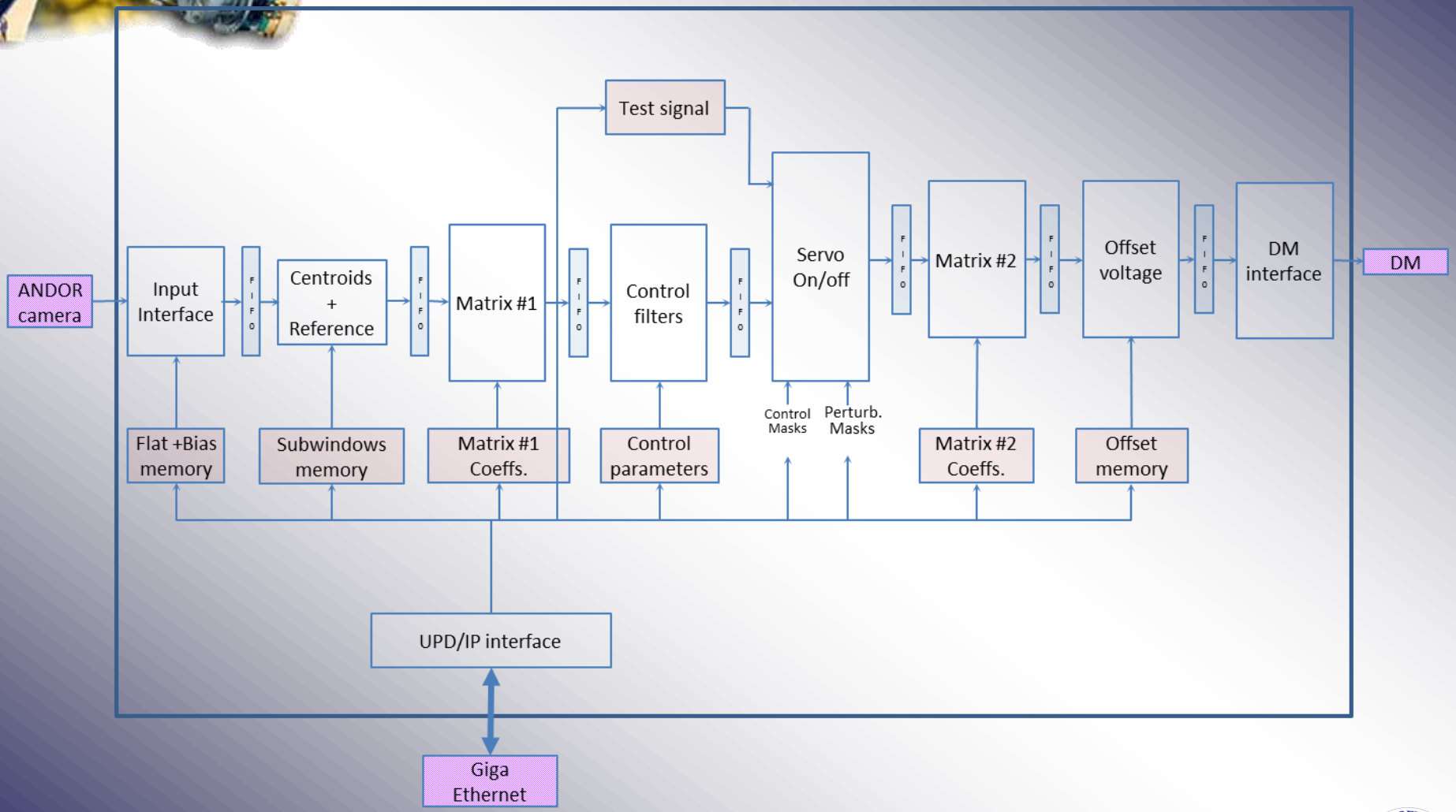
EDiFiSE RTC physical block diagram

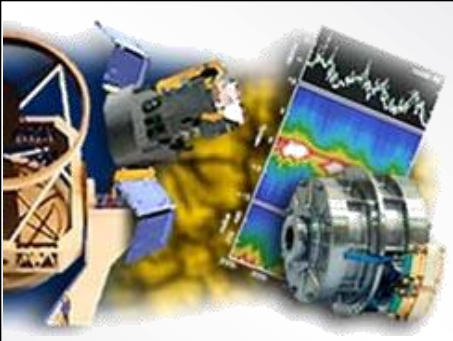


- 500 Hz
- 16x16 SH WFS
- 97 actuators

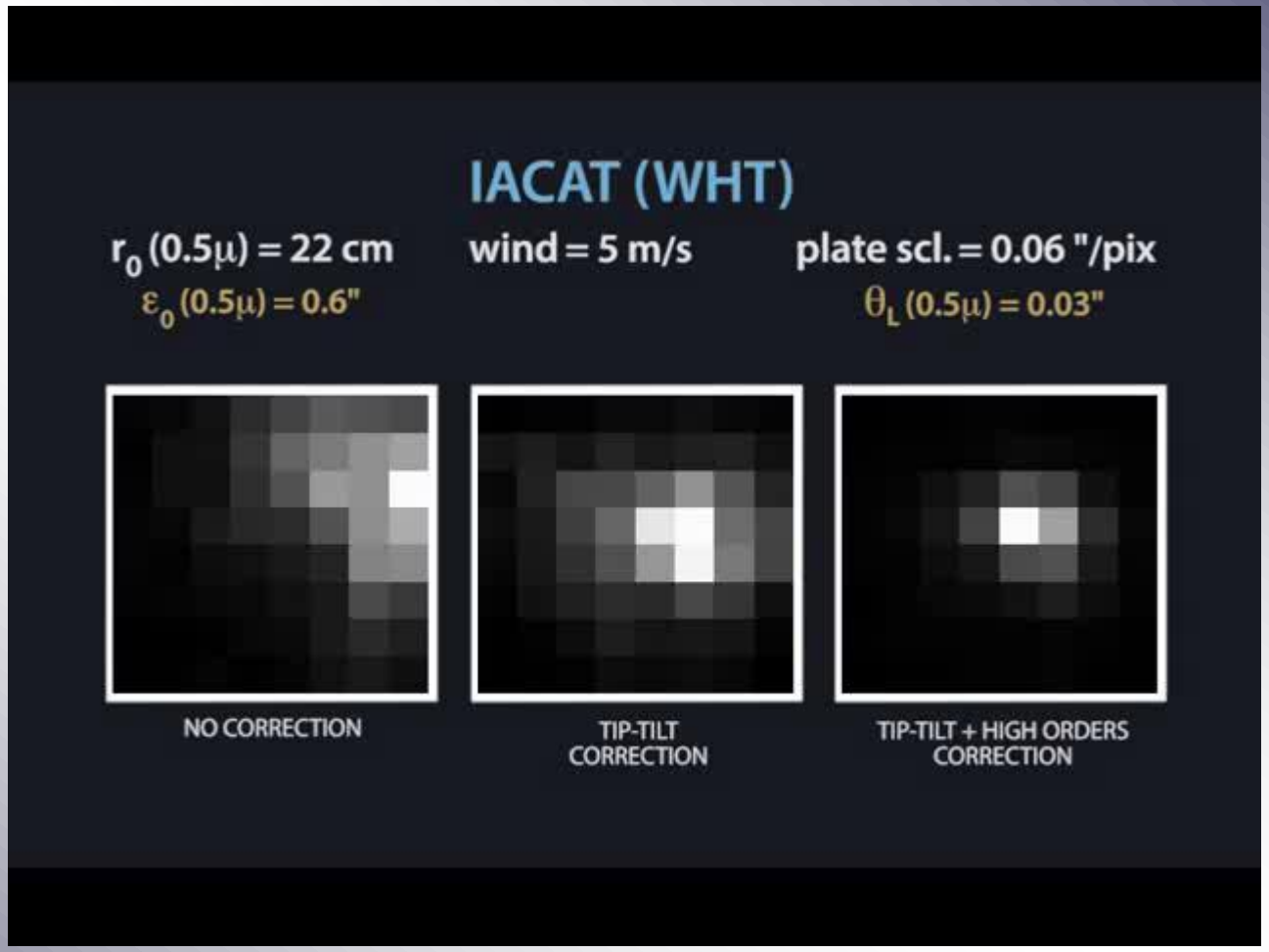


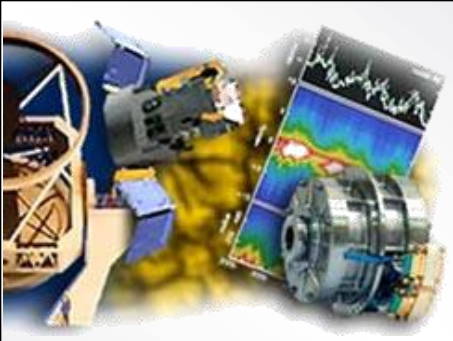
EDiFiSE FPGA RTC



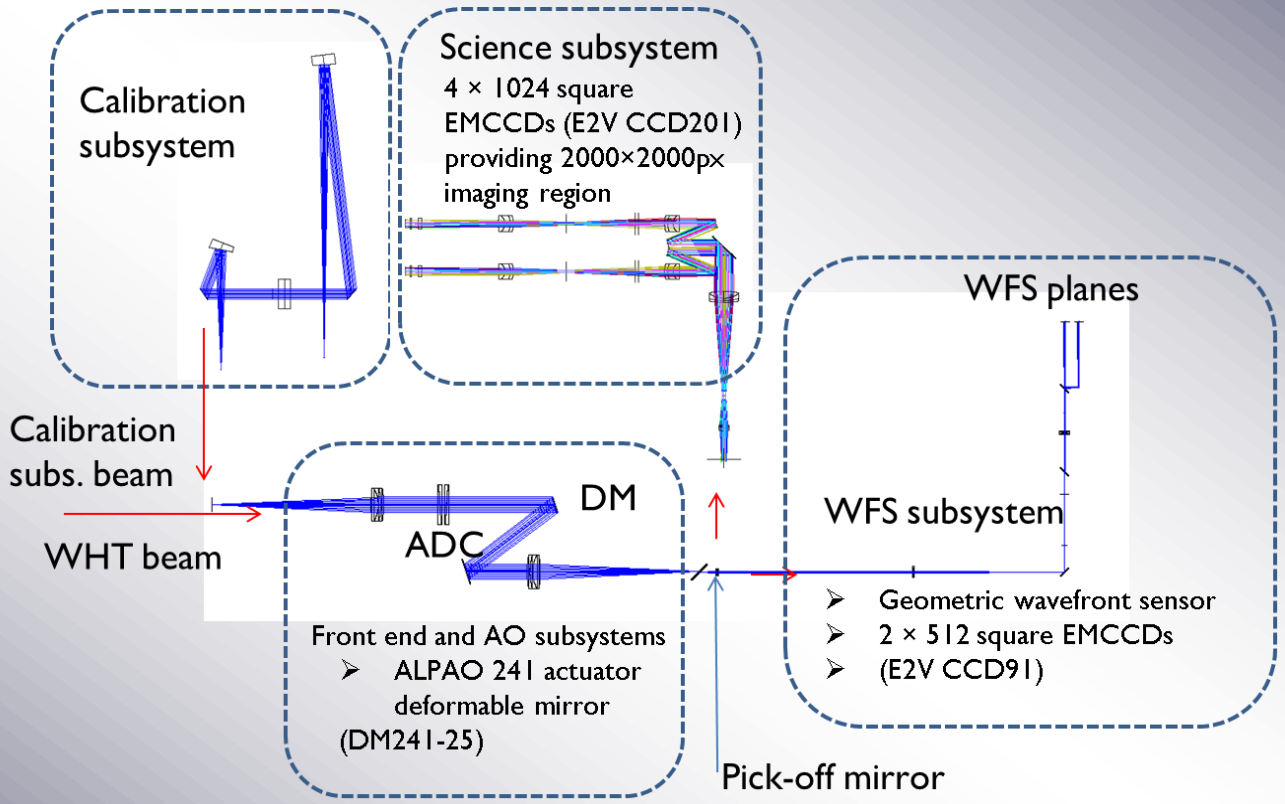


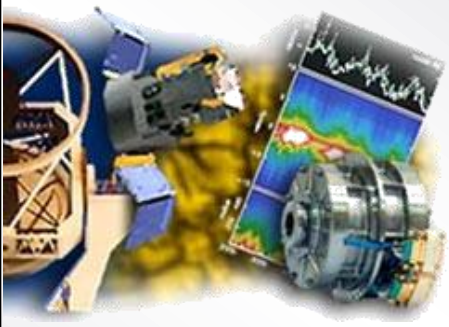
EDiFiSE Movie



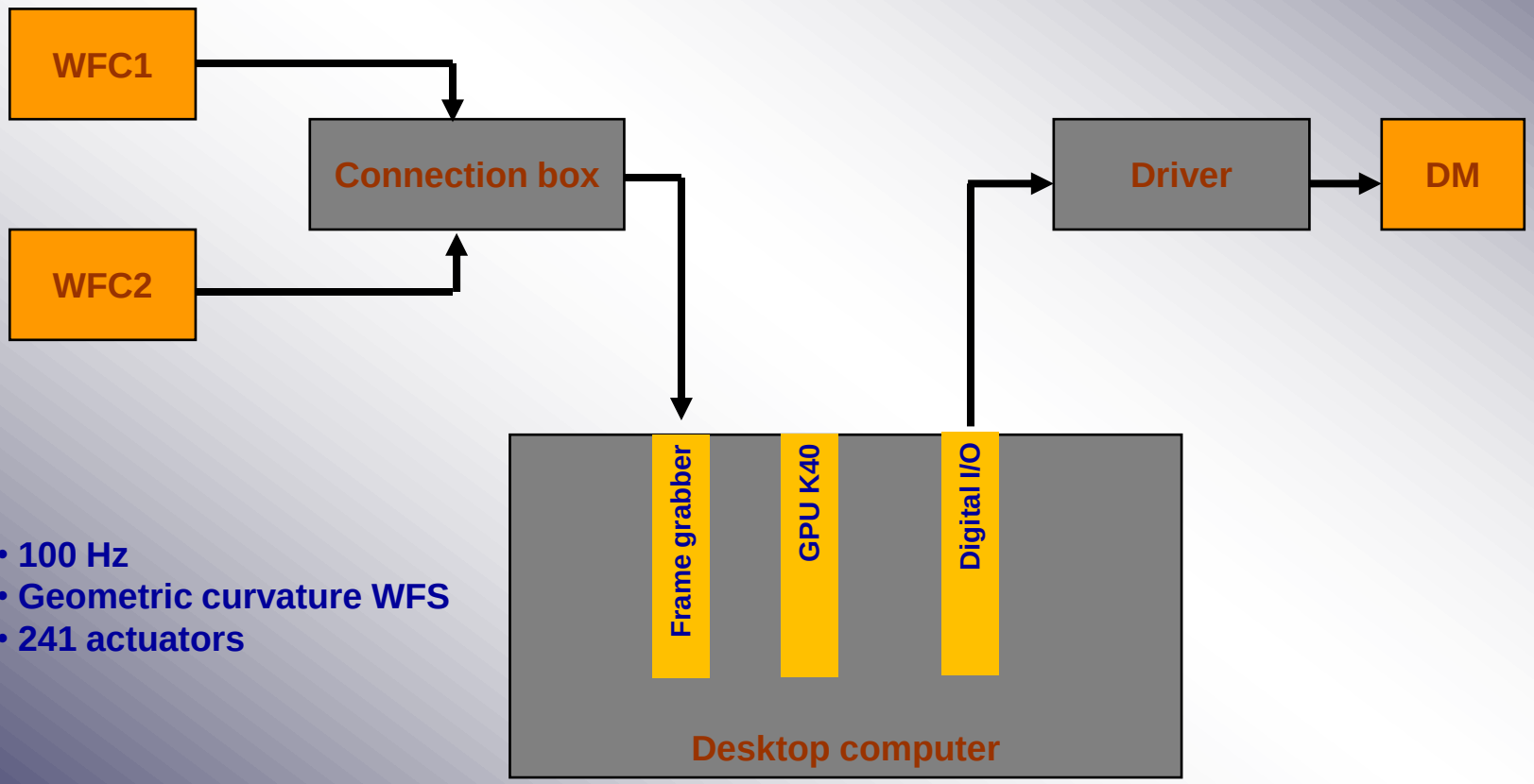


AOLI

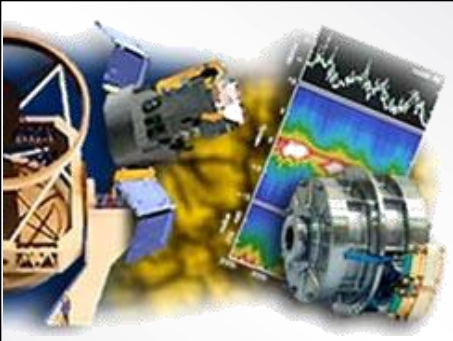

Calibration subsystem
Science subsystem
4 × 1024 square EMCCDs (E2V CCD201) providing 2000×2000px imaging region
WFS planes
Calibration subs. beam
WHT beam
DM
ADC
WFS subsystem
Geometric wavefront sensor
2 × 512 square EMCCDs
(E2V CCD91)
Front end and AO subsystems
ALPAO 241 actuator deformable mirror (DM241-25)
Pick-off mirror



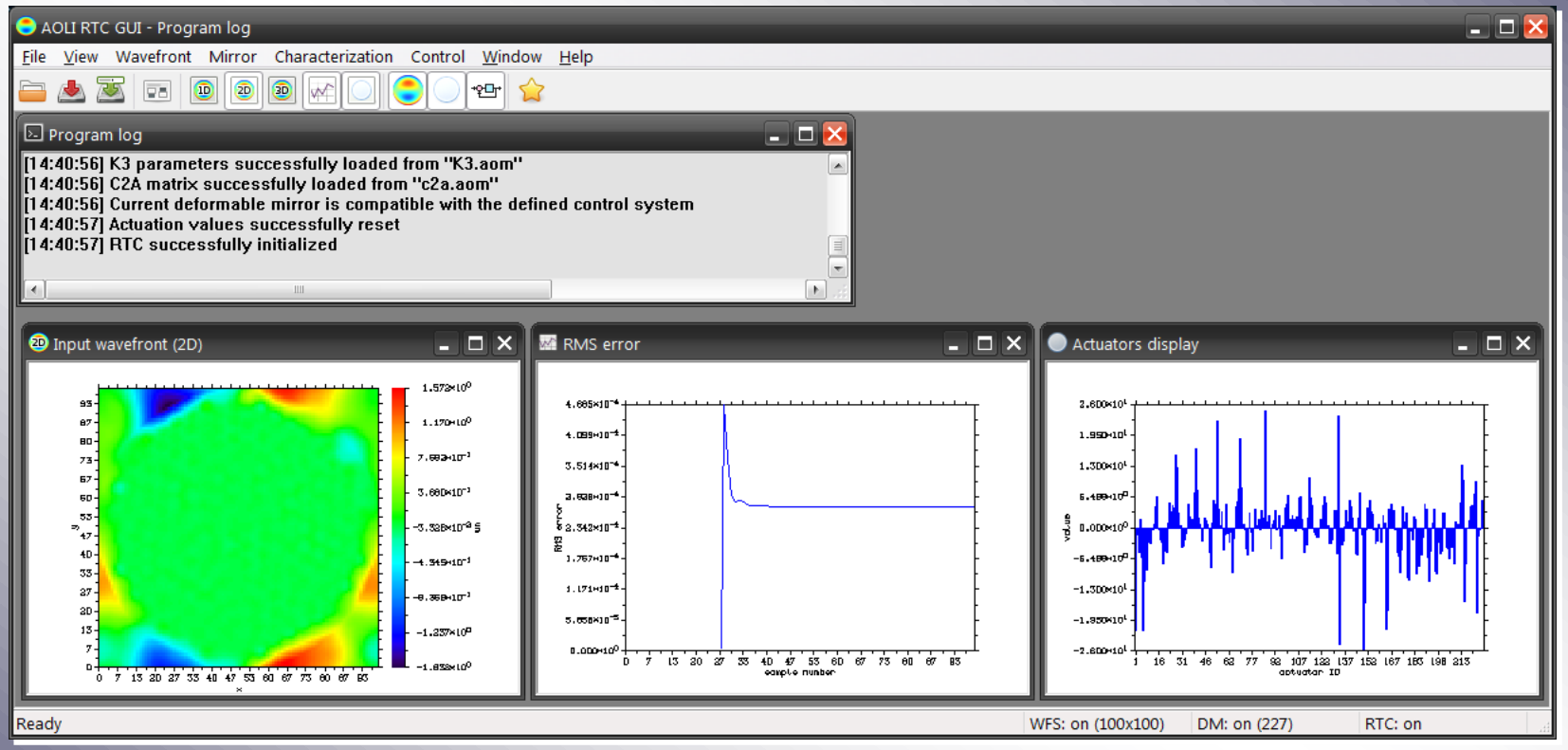
AOLI RTC physical arrangement

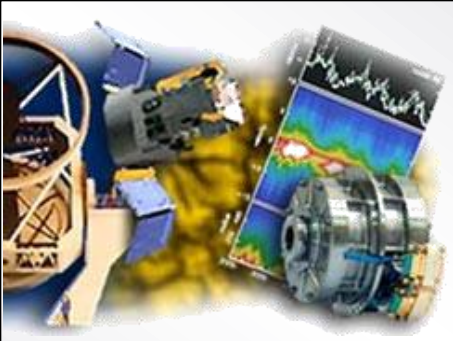


- 100 Hz
- Geometric curvature WFS
- 241 actuators

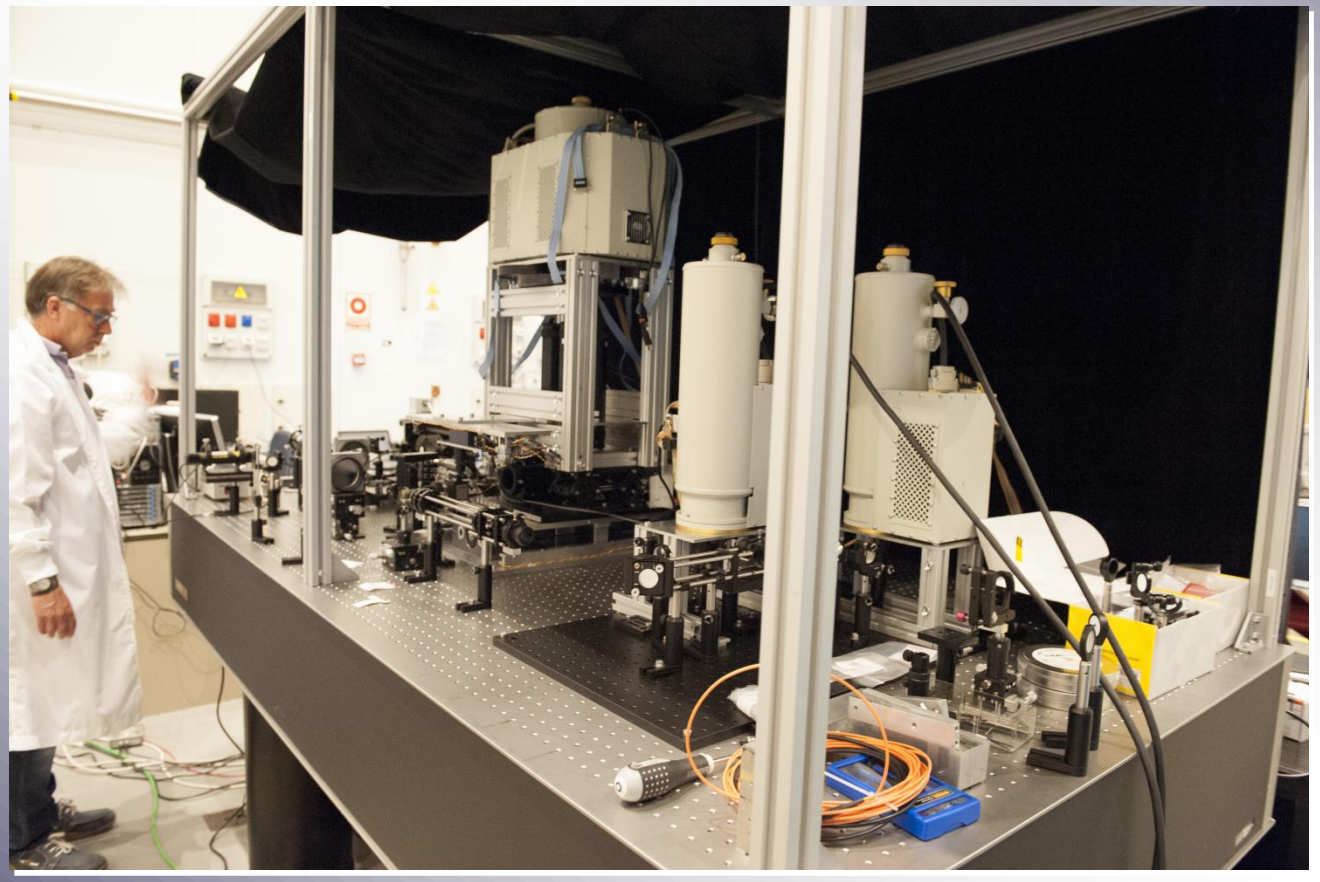


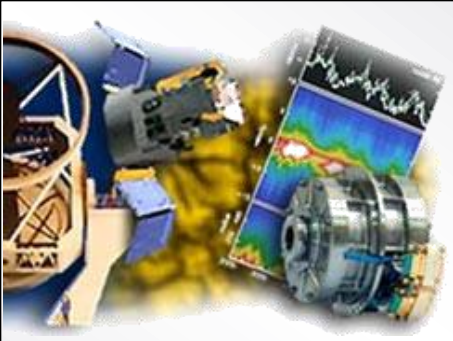
AOLI GUI


AOLI RTC GUI - Program log
File View Wavefront Mirror Characterization Control Window Help
Program log
[14:40:56] K3 parameters successfully loaded from "K3.aom"
[14:40:56] C2A matrix successfully loaded from "c2a.aom"
[14:40:56] Current deformable mirror is compatible with the defined control system
[14:40:57] Actuation values successfully reset
[14:40:57] RTC successfully initialized
Input wavefront (2D)
RMS error
Actuators display
Ready
WFS: on (100x100)
DM: on (227)
RTC: on

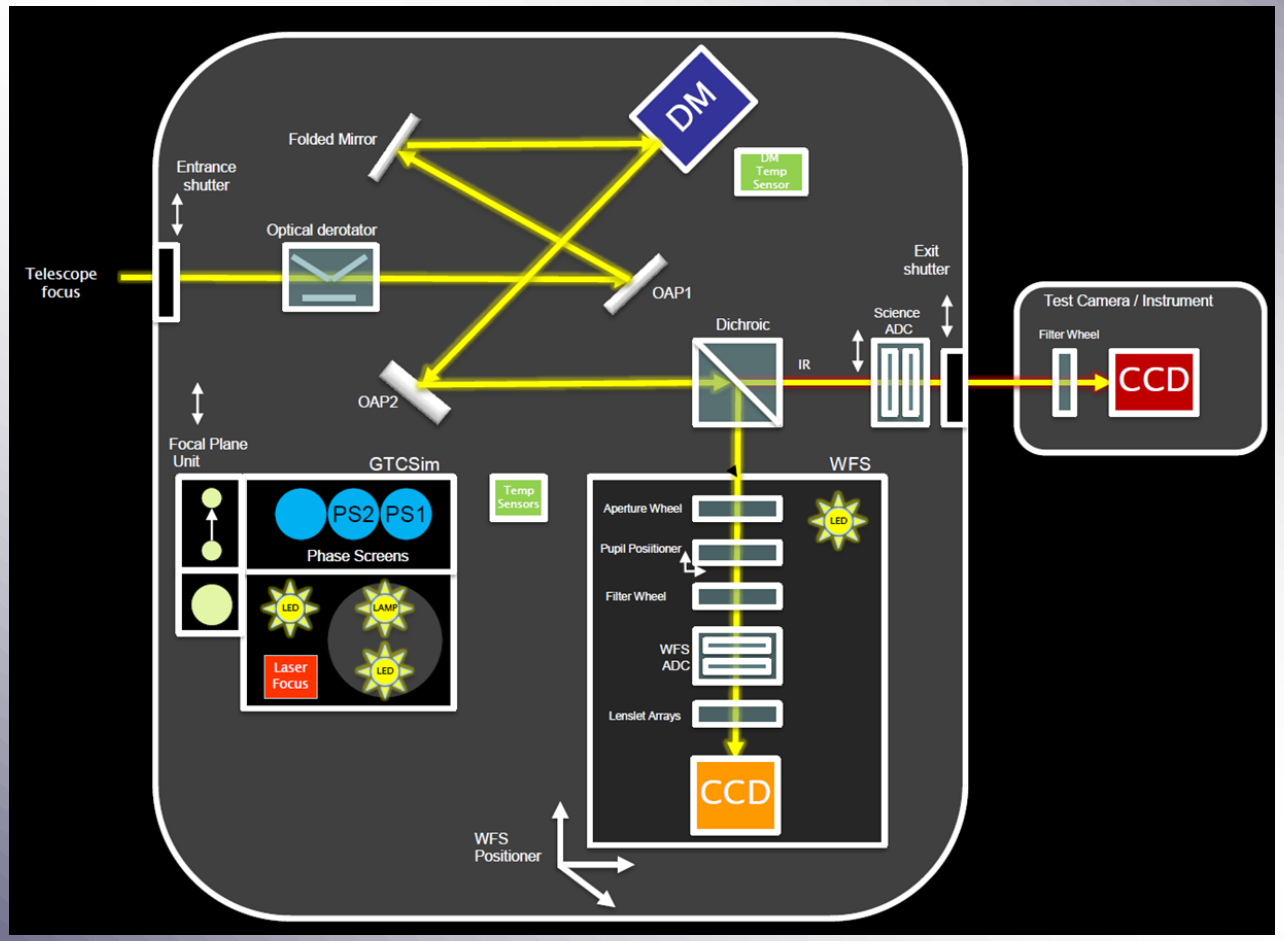


AOLI Laboratory testing

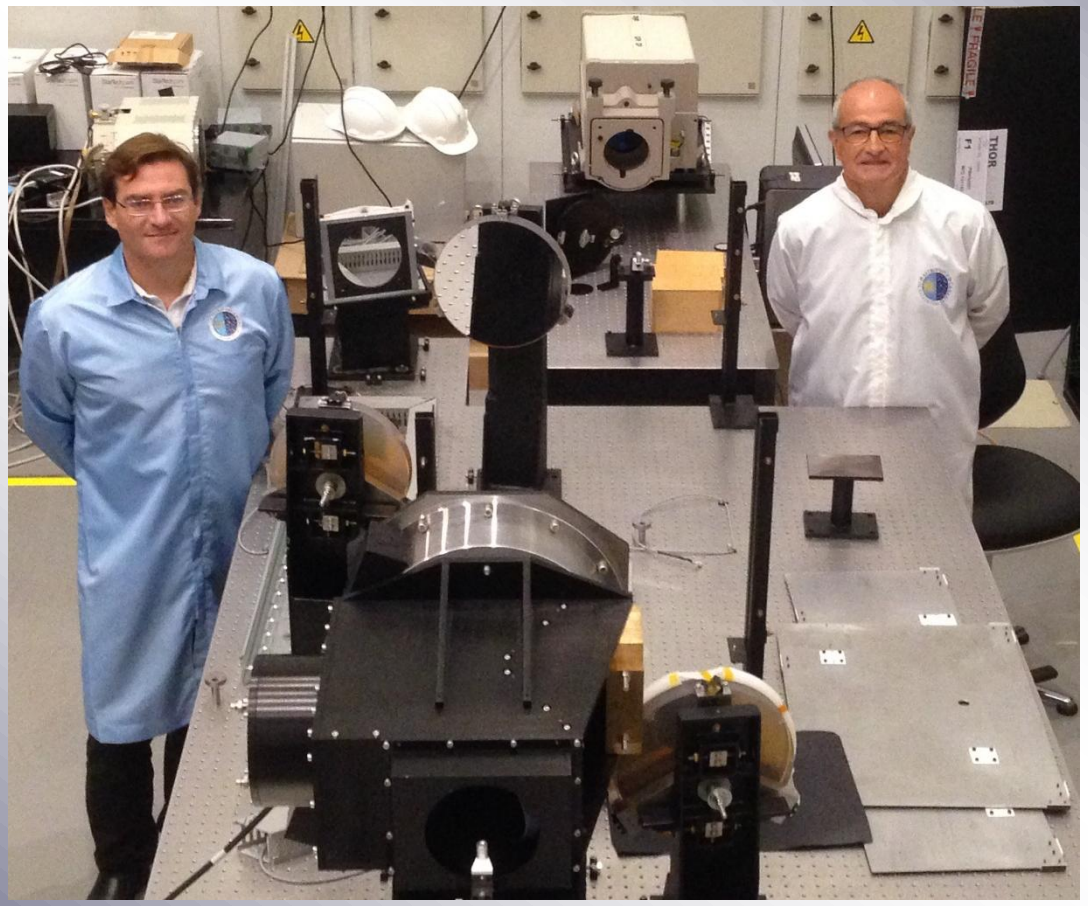


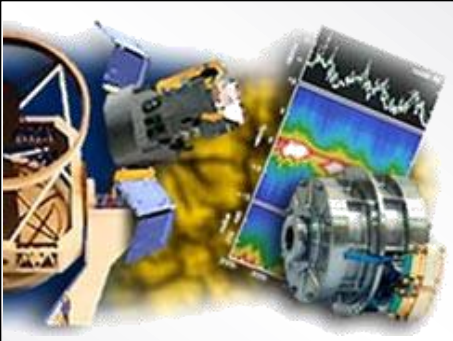


GTCAO

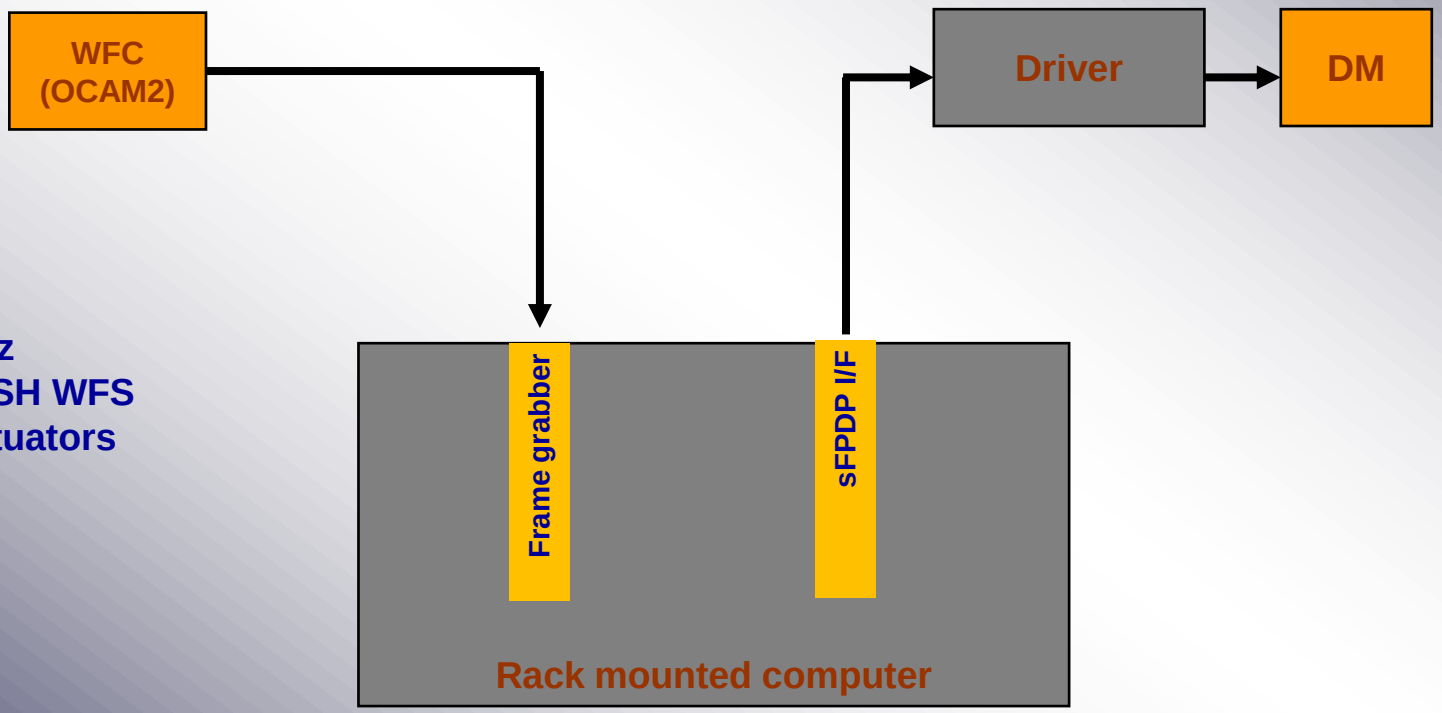

DM
Folded Mirror
DM Temp Sensor
Entrance shutter
Optical derotator
Telescope focus
OAP1
Exit shutter
Test Camera / Instrument
Filter Wheel
CCD
Dichroic
Science ADC
IR
OAP2
Focal Plane Unit
GTCSim
PS2
PS1
Phase Screens
LED
LAMP
LED
Laser Focus
Temp Sensors
WFS
Aperture Wheel
Pupil Positioner
Filter Wheel
WFS ADC
Lenslet Arrays
LED
CCD
WFS Positioner

GTCAO Laboratory integration

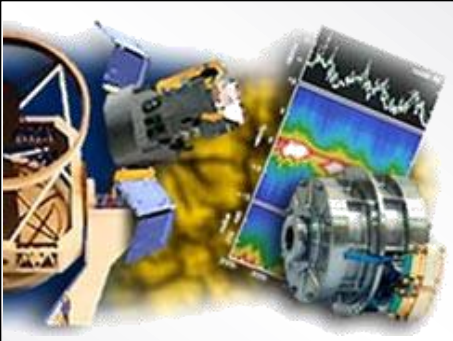




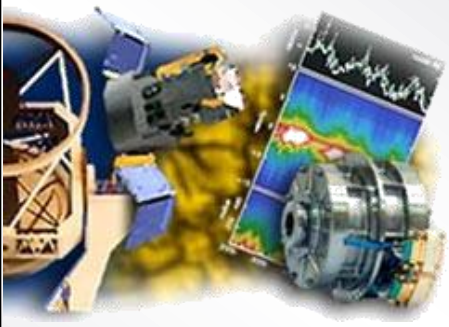
GTCAO RTC block diagram



- 1500 Hz
- 20x20 SH WFS
- 373 actuators

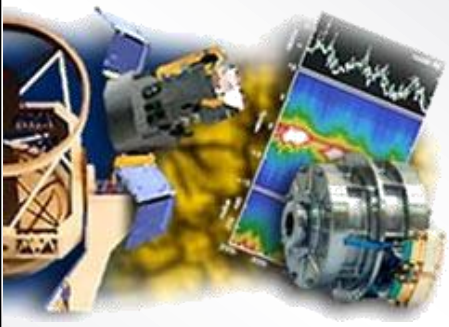


Contents



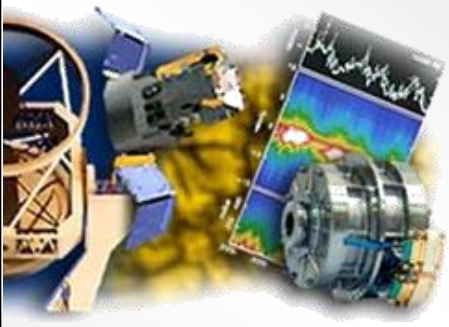
FPGA

- "Field programmable gate arrays", FPGA
- Raw silicon ready to be configured by the programmer. No fixed core.
- Truly parallel
- Virtually any combination of operations
- Low-level programming, some high level translators available.



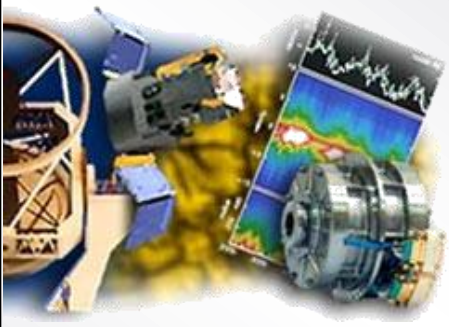
GPU

- “Graphics Processing Units”, GPU
- Very fast processing of relatively simple tasks
- Performed frame buffer intended for immediate display
- Parallel structure, plenty of processors
- CUDA, OpenCL

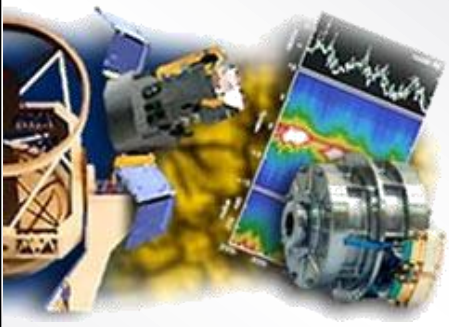


CPU

- “Central Processing Units”, CPU
- Well known and widespread
- Processing power permanently growing
- Carries out the instructions of a sequential computer program
- Many cores available
- C, C++, python high level programming

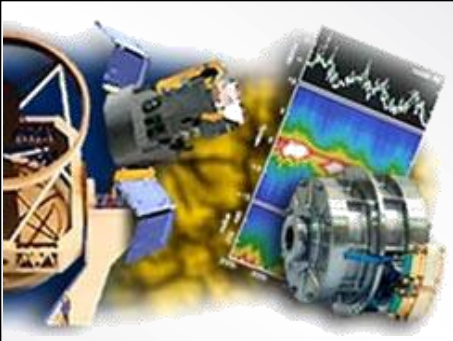


Contents



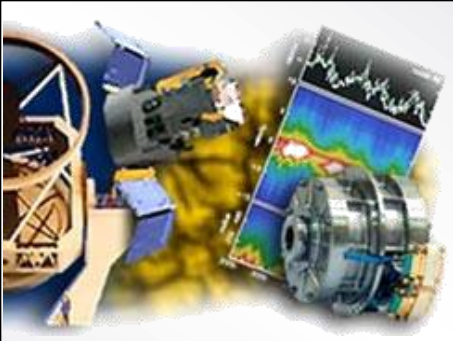
Hardware cost

"The cost of the hardware required for the execution of the algorithms"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
A couple of general purpose development boards: ≈3 K€	Desktop PC, highly equipped, plus K40 GPU board: ≈9 K€	Rack-mounted PC, highly equipped in both memory and disk: ≈5 K€
👍	👎	≈



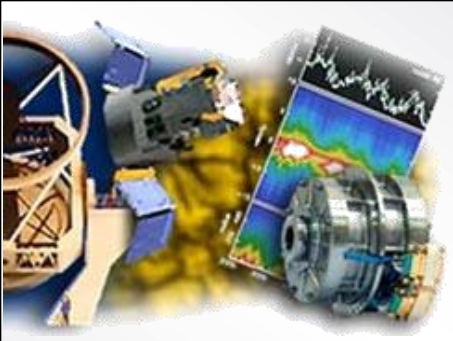
Development cost

"Engineering effort required for the development of the real-time control system"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
Estimated 3 engineer-year, including the subcontract of part of the FPGA development.	Estimated 2 engineer-year, including both GPU program and CPU control	Estimated 1 engineer-year, making full re-use of available software
👎	≈	👍



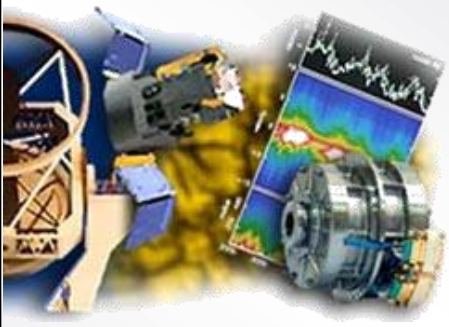
Skill level

"required background of the developing engineers "		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
High level of VHDL design knowledge is required, not easily found. A background in electronics is preferable.	C and C++ under Linux programming experience required, plus CUDA.	C, C++ and python programming experience required, under Linux.
👎	≈	👍



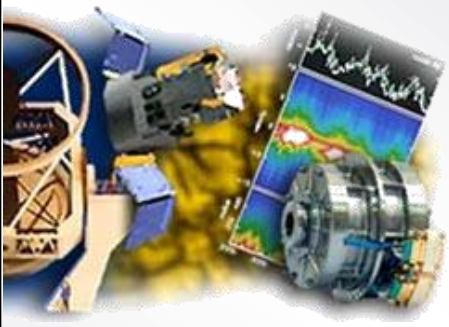
Flexibility

"Capability of the system for accepting changes, specifically in code"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
Any change in the system requires the synthesis of the new code, which can take dozens of minutes and may present design problems.	Software change only requires compilation and building.	Software change only requires compilation and building.
👎	👍	👍



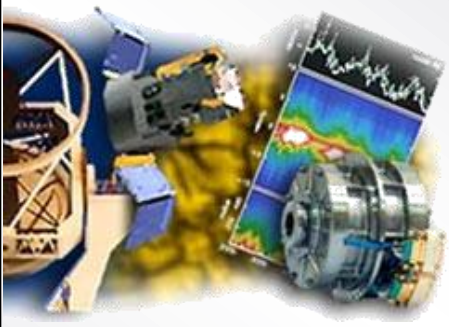
Reusability

"using already developed and tested, ready to use, existing code instead of developing and verifying new pieces"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
Design in the VHDL field is normally based on reusable IP modules.	CUDA programs are specific to NVIDIA GPU boards, but there are many of them available.	CPU real-time control is making full use of available software.
👍	≈	👍



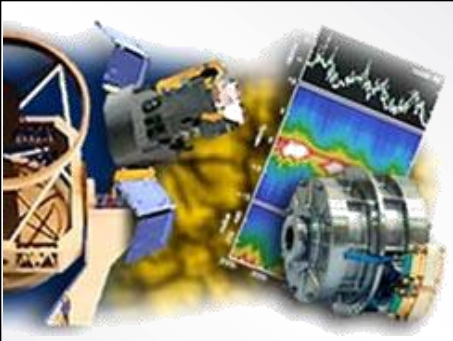
Latency

"time elapsed since the arrival of the last pixel from the camera to the availability of the actuation command"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
Latency in the FPGA processing is really low, due to the intrinsically parallel nature of the logic. Less than 10% of loop time (~150 µs)	Key figure for latency is the "bottleneck" of the delivery of the images to the GPU (~2ms). However, it can be accepted due to the relative low speed of this loop (100 Hz)	The processing can be broken down among many threads and cores, minimising latency. It has been estimated to ~250 µs
👍	👎	≈



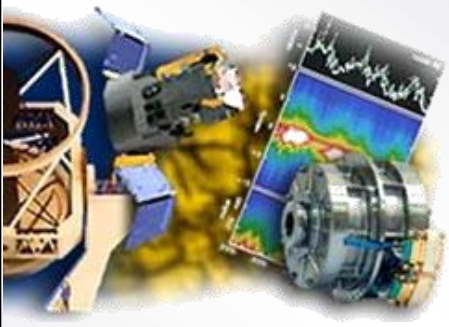
Jitter

"variation in the latency"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
The FPGA logic is completely deterministic and its state can be known down to every clock cycle. Jitter is thus negligible.	GPU processing is virtually jitter-free, but the operating system (Linux) is running all time. Jitter peaks of several iterations are common.	The use of a real-time Kernel provides a reasonably low jitter behaviour. Jitter peaks of several iterations can be observed.
👍	👎	≈



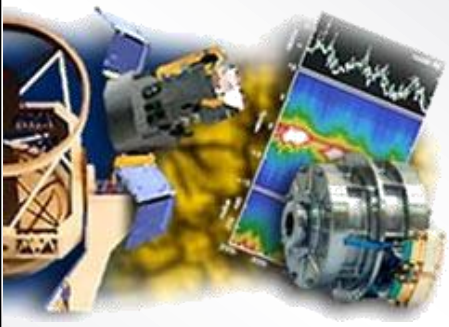
Power consumption

"power consumed by the computing hardware"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
Power consumption of FPGA itself and related logic, can be estimated in the really low figure of 4 watts.	The power consumption directly related to the CPU processor can be estimated in 100 watts. GPU board is specified at 235 W.	As already cited in the AOLI case, the CPU related power consumption is in the order of 100 W, depending on the number of cores being used.
👍	👎	👎



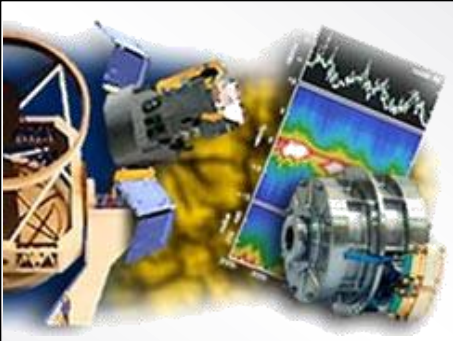
Volume

"physical volume associated to processors"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
A 1U 19" rack is enough for allocating both the low-order and the high-order processing FPGAs	A desktop PC computer, with extra powerful power supply, has been selected for allocating the GPU board and frame grabbers.	A 4U, 19" rack mounted PC, short depth, has been used for the allocation of all processors and frame grabbers.
👍	👎	👎



Weight

"weight associated to processors"		
EDiFiSE (FPGA)	**AOLI** (GPU+CPU)	**GTCAO** (CPU)
A fairly simple PCB board is enough for the computation and servicing of the real-time loop. A Xilinx general purpose board weighting a few hundred grams is used.	The rack mounted which allocates the K40 GPU board weights 13 Kg. The GPU board is specified at 826 gr.	The use of a highly featured PC computer, rack mounted, as previously said for the AOLI case, is in the order of 13 Kg, two orders of magnitude greater than the FPGA case.
👍	👎	👎



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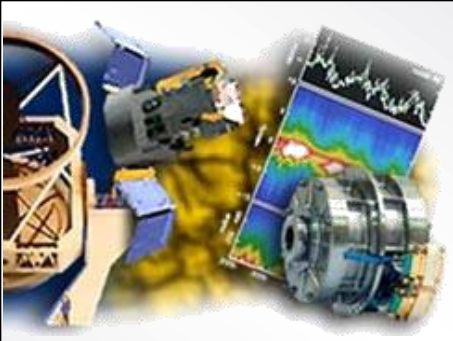
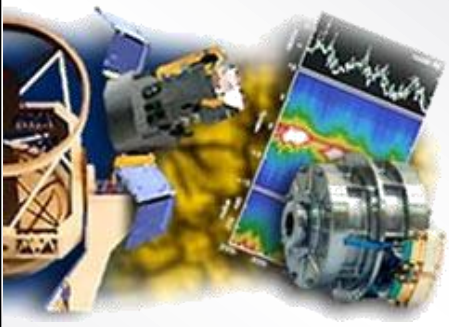


Conclusions

- Each technology has pros and cons
- No absolute winner can be identified
- Instead, every development should make its own assessment



Thanks!