Green Flash

Adaptive Optics real-time control at ELT scales

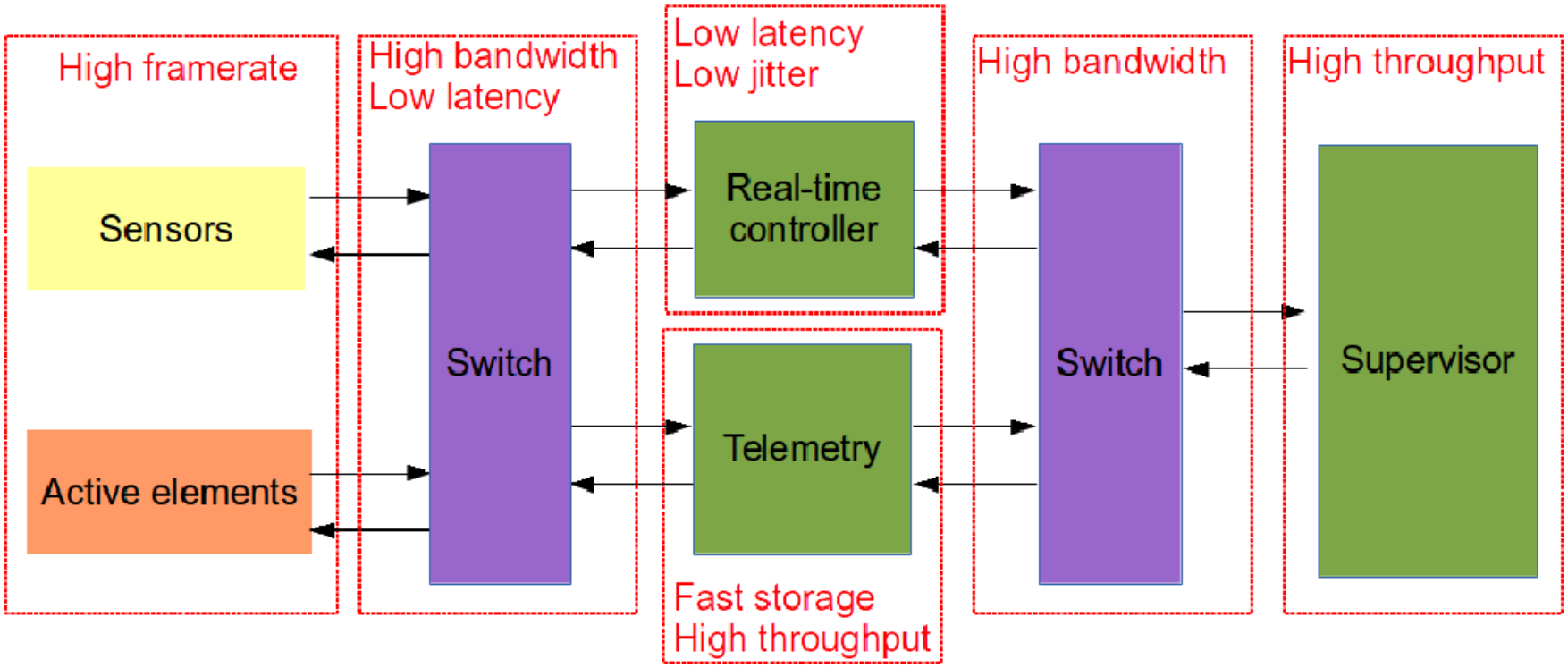
AO RTC workshop
Paris, 26 January 2016

Project #671662 funded by European Commission under program H2020-EU.1.2.2 coordinated in H2020-FETHPC-2014

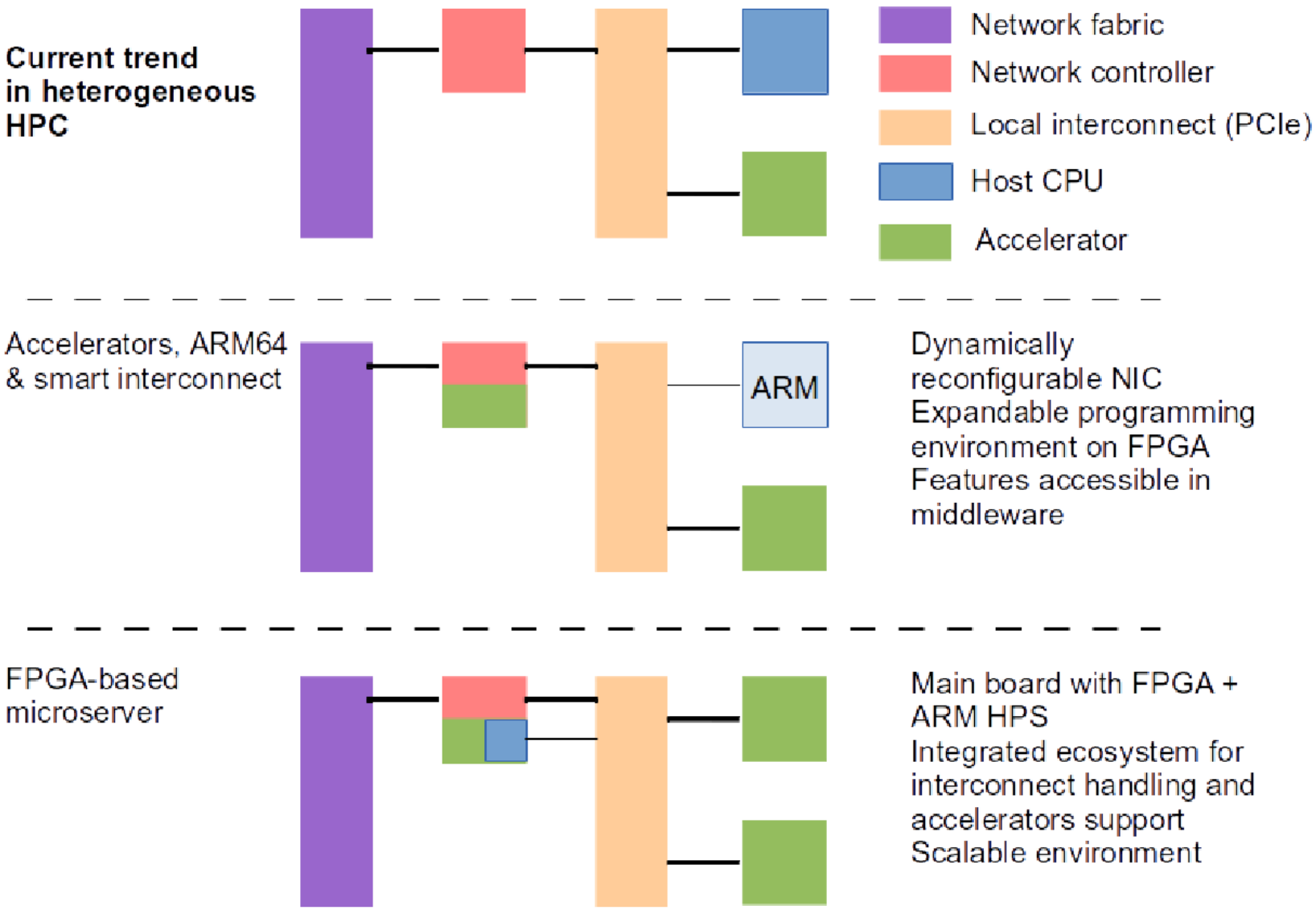
Introduction to Green Flash

- Program objectives: 3 research axes
  - 2 technological developments and 1 validation study
- Real-time HPC using accelerators and smart interconnects
  - Assess the determinism of accelerators performance
  - Develop a smart interconnect strategy to cope for strong data transfer bandwidth constraints
- Energy efficient platform based on FPGA for HPC
  - Prototype a main board, based on FPGA SoC and PCIe Gen3
  - Cluster such boards and assess performance in terms of energy efficiency and determinism
- AO RTC prototyping and performance assessment
  - Assemble a full functionality prototype for a scalable AO RTC targeting the MAORY system
  - Compare off-the-shelf solutions based on accelerators and new FPGA-based concept

AO RTC concept

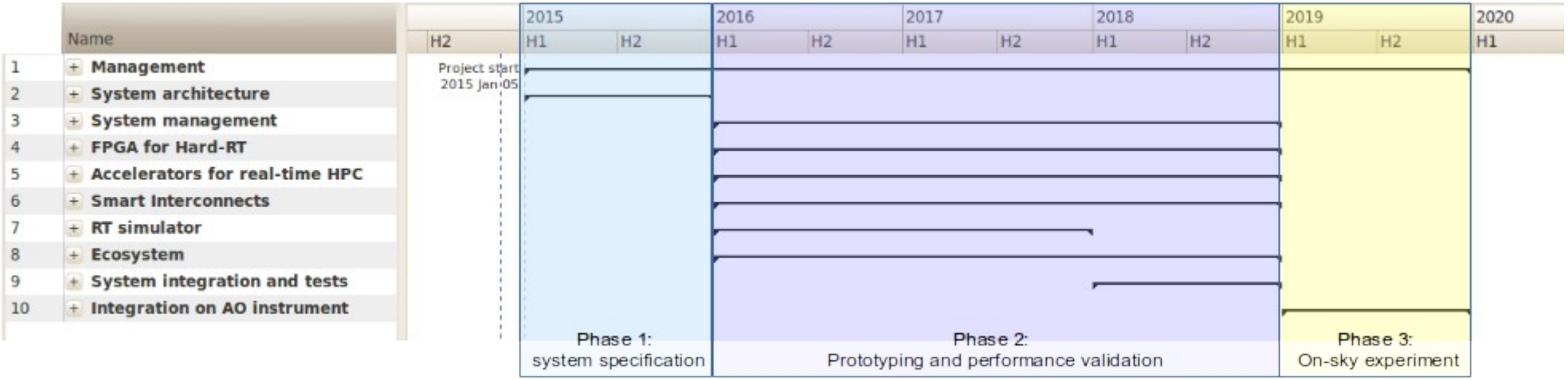


Assessing new HPC concepts



Project Management

- 3 phases. Entering Phase 2, funded through H2020 program
  - Main prototyping phase from systemm specifications
  - On-sky experiment to be defined along the course of the project



Partnership

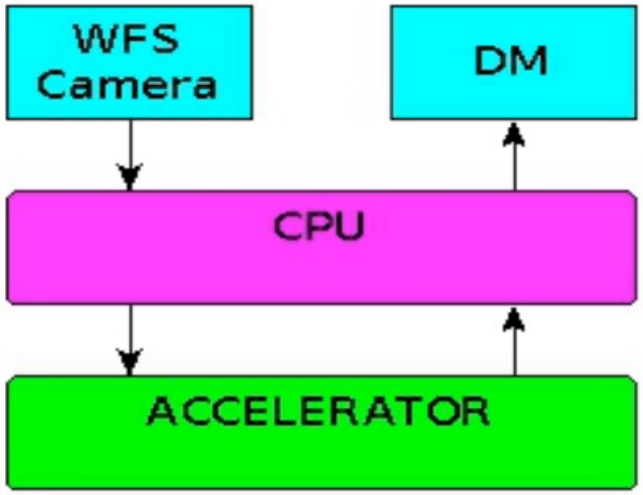
- 2 academic partners
  - LESIA, Observatoire de Paris
    - Large experience in AO design and integration, high performance AO simulation on GPUs, enabling technologies for accelarator based RTC
  - University of Durham
    - Significant contribution to SPARTA, large experience on AO RTC design integration : DARC
  - Ongoing collaboration : CANARY demonstrator
- 2 partner SMEs
  - Microgate
    - History of developments in wavefront controllers (Keck, MMT, LBT) and ASM / DSM (VLT, LBT, E-ELT)
  - PLDA
    - French SME specialized in FPGA developments (boards, IPs, development environment), industry leader in PCIe Ips.
- 3.8 M€ budget over 3 years for the prototyping phase

Interaction with external partners

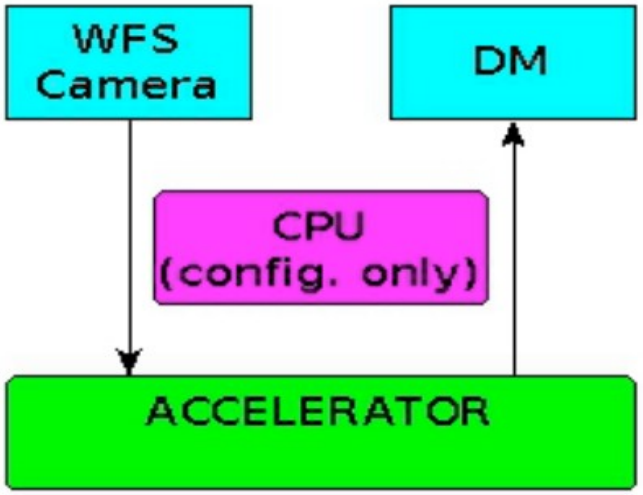
- Collaboration with HPC partners
  - MORSE project on optimized linear algebra
  - Other possible partners : e.g. around OmpSs developed at BSC
- Follow up on E-ELT instruments design specifications
  - After PDR, mid-term review
  - Welcome interactions as much as possible
- Follow up on ESO standard definition as they become public
  - Welcome interactions as much as possible

Technology down selection

- Mainstream technologies versus emerging technologies
  - Hardware accelerators (GPU, Xeon Phi) versus CPU versus FPGA



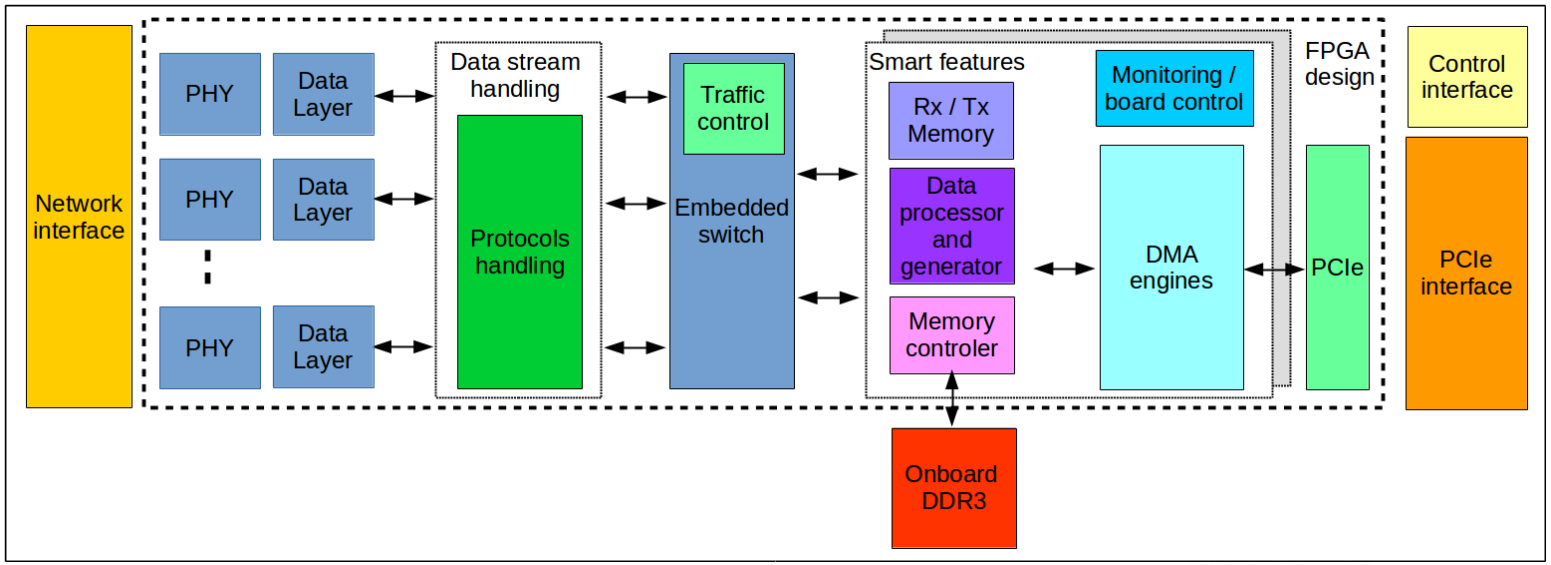
Accelerator Data Flow



Embedded Data Flow

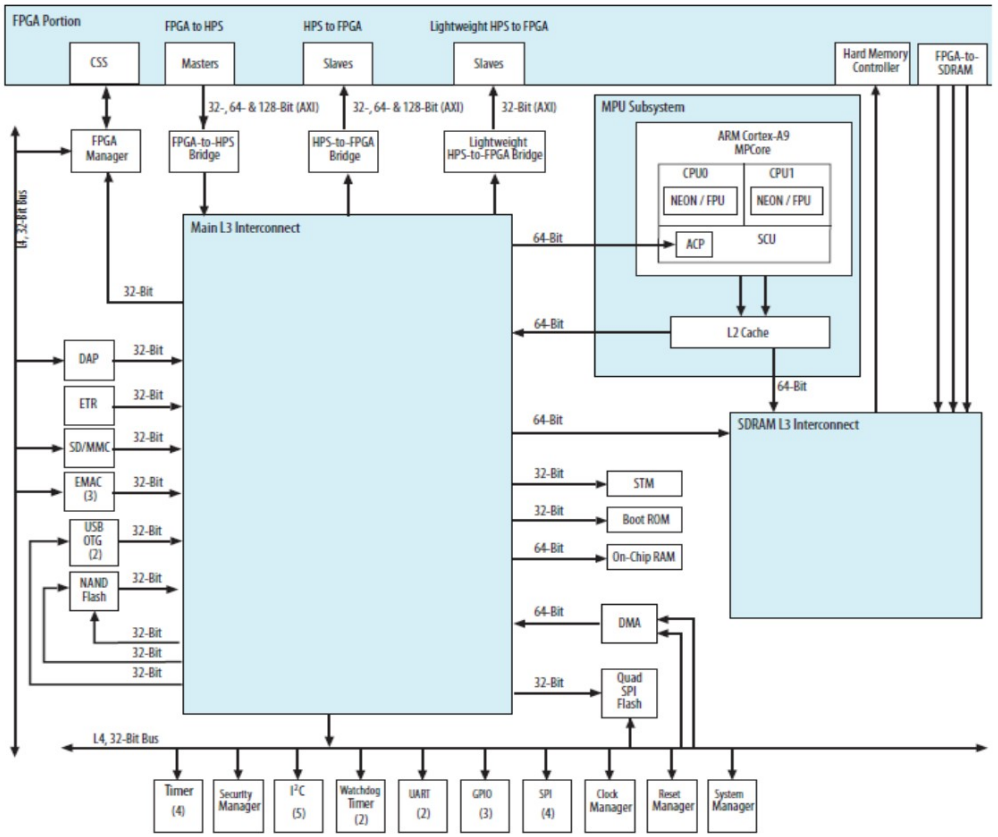
Central development : smart interconnect strategy

- Required to cope for various specifications
  - High Throughput in the supervisor module over distributed memory architecture
  - Low latency data acquisition from sensors
  - Possible distributed architecture for the real-time data pipeline



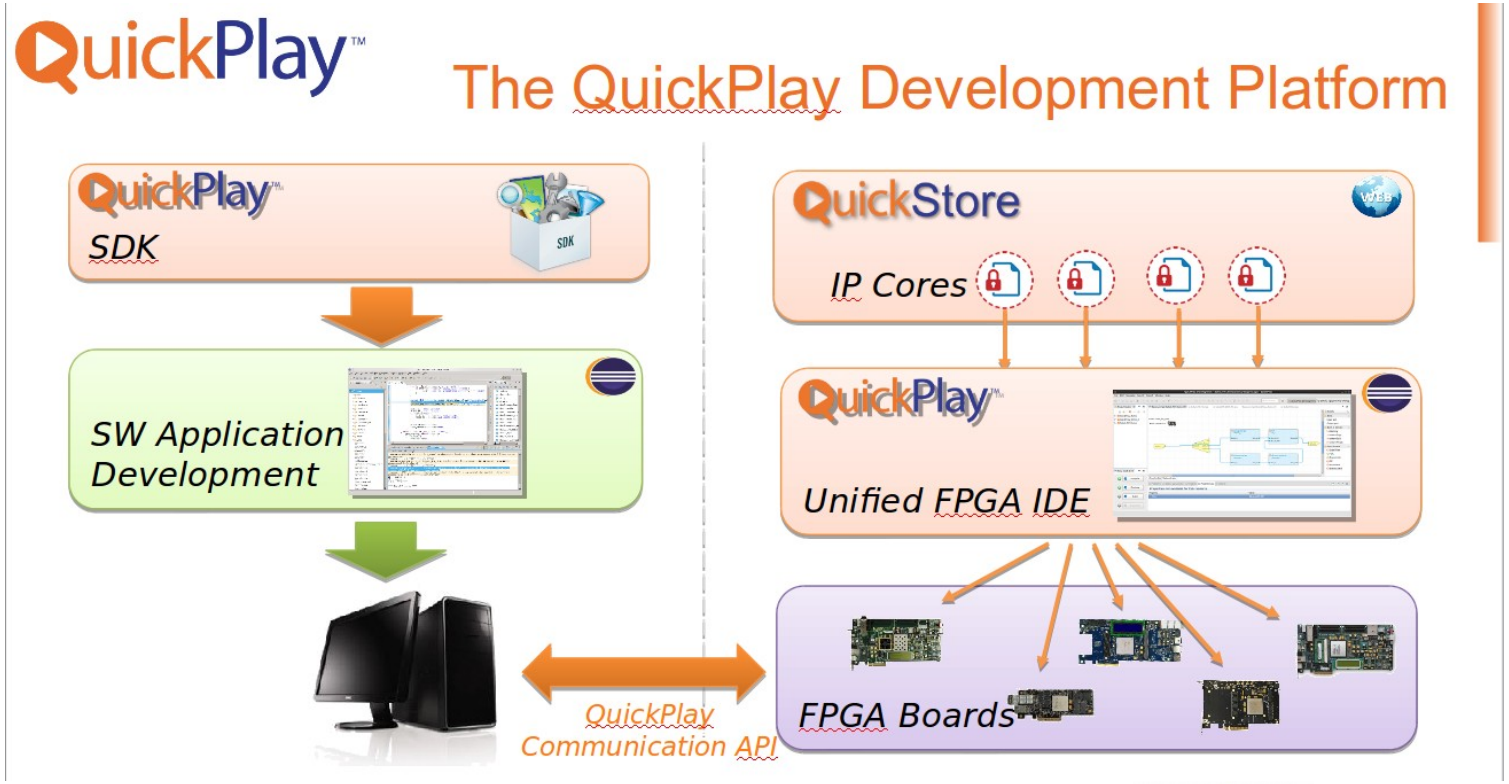
Central development : FPGA for hard real-time

- Custom development at Microgate
  - High cell density FPGA from Altera : Arria 10
  - On board ARM HPS
  - Several dimensioning to cope for requirements on com. and compute
  - Several board designs explored hosting one or several FPGAs



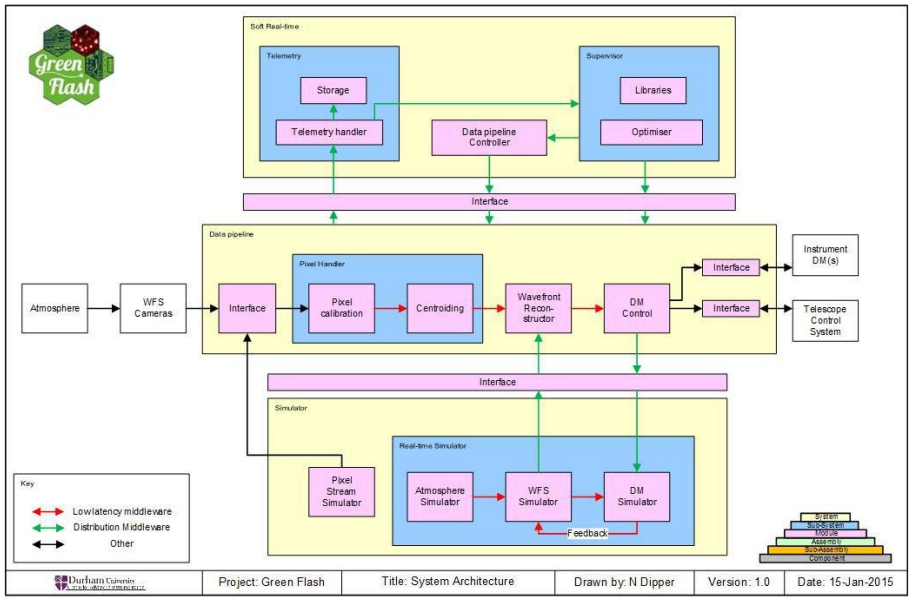
Enabling technology : QuickPlay

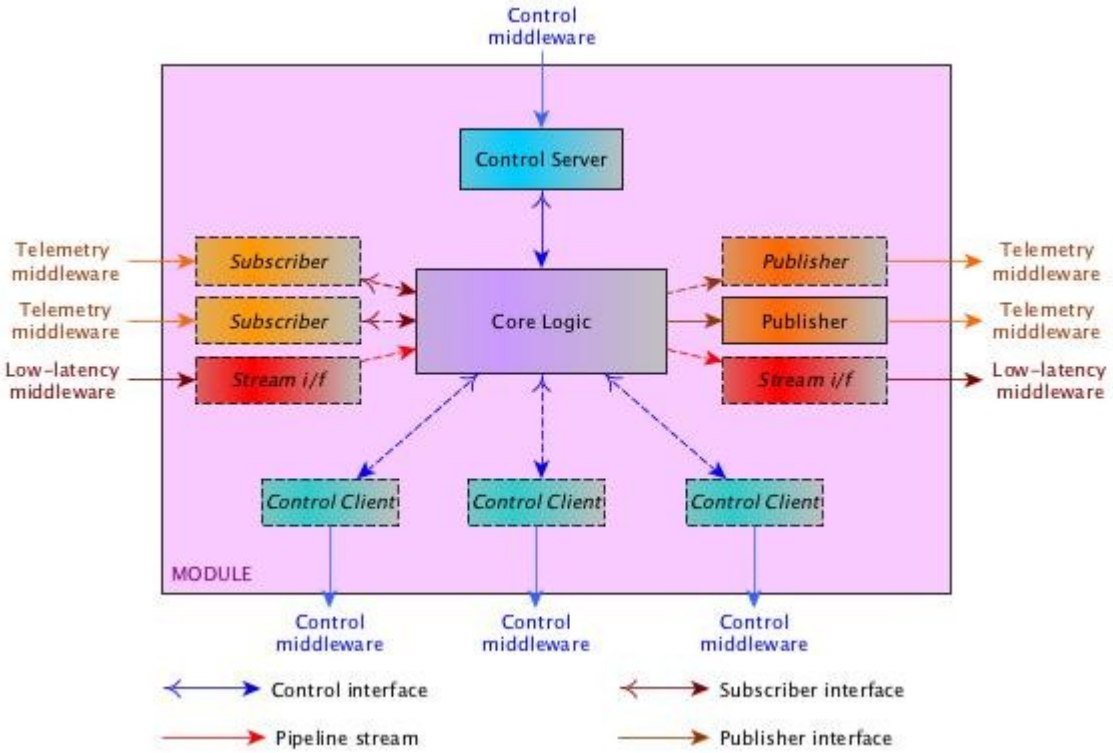
- Allow fast development of FPGA applications
  - Optimized HLS : integration of compute blocks (C based) with dedicated IPs (UDP / Ethernet, PCIe, etc …)



Middleware strategy

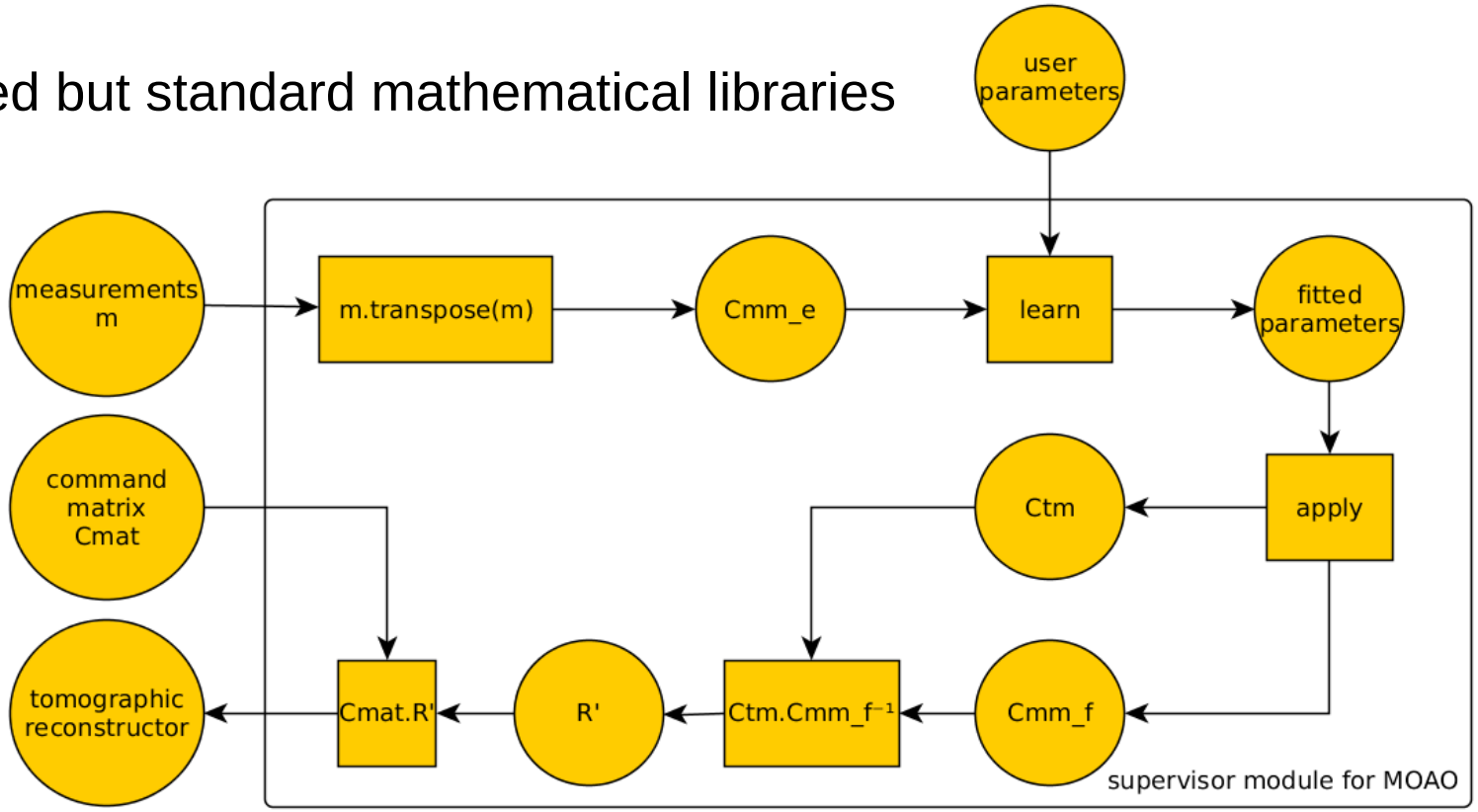
- Developed at Durham, based on DDS
  - High level of abstraction from the hardware : portable / reusable code





Supervisor strategy

- Targeting MCAO on an E-ELT
  - Compute the command matrix requires the inversion of a large ~100k x 100k matrix
  - Use optimized but standard mathematical libraries



Maintainability & obsolescence

- Two critical parameters in this technology down selection
- Solution to both is to be able to abstract the software from the hardware
- Not an easy task when targeting real-time applications
- In Green Flash :
  - use of standard libraries, C++, CUDA or OpenCL (C based, few specific keywords, easy to migrate)
  - use of a comprehensive FPGA development environment (joint develoment of FPGA design, firmware, driver and higher level API for user)
  - Middleware with high level of abstraction (DDS based)
- Other critical aspect : address data transfer over the whole system
  - Need for a tailored solution
  - Smart interconnect concept : unified reconfigurable high performance interconnect

Conclusion

- Large technological trade off study
- Emerging technologies on the HPC market
- Targeting the prototyping of a RTC for a MCAO system on the E-ELT
- 4 partners (2 academic, 2 SMEs), about 4M€ budget, 3 years development plan
- … and a lot of fun