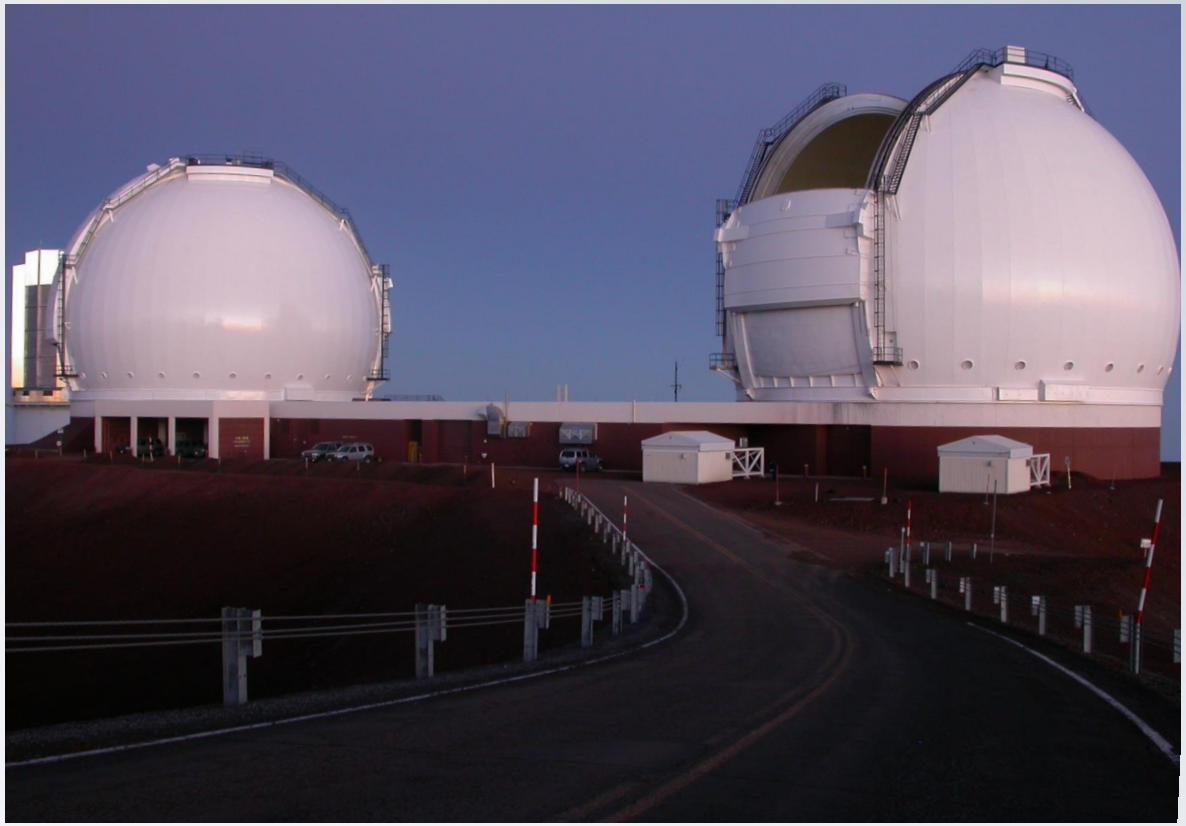


The new RTC system for Keck AO

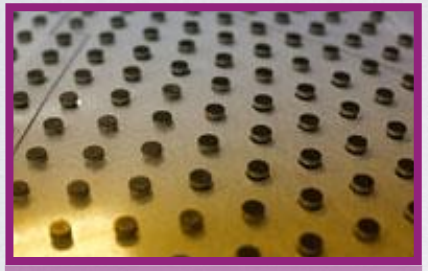
Roberto Biasi - Microgate

Outline

- Company presentation - ultrashort
- Background
- Keck RTC RFP, planning, requirements
- Keck RTC preliminary design
- Conclusions

MICROGATE

MICROGATE



Engineering

Advanced control systems for adaptive optics and telescopes

Professional Timing

Professional timing equipment for sports

Training & Sport

Athletic performance evaluation systems

Medical Rehab

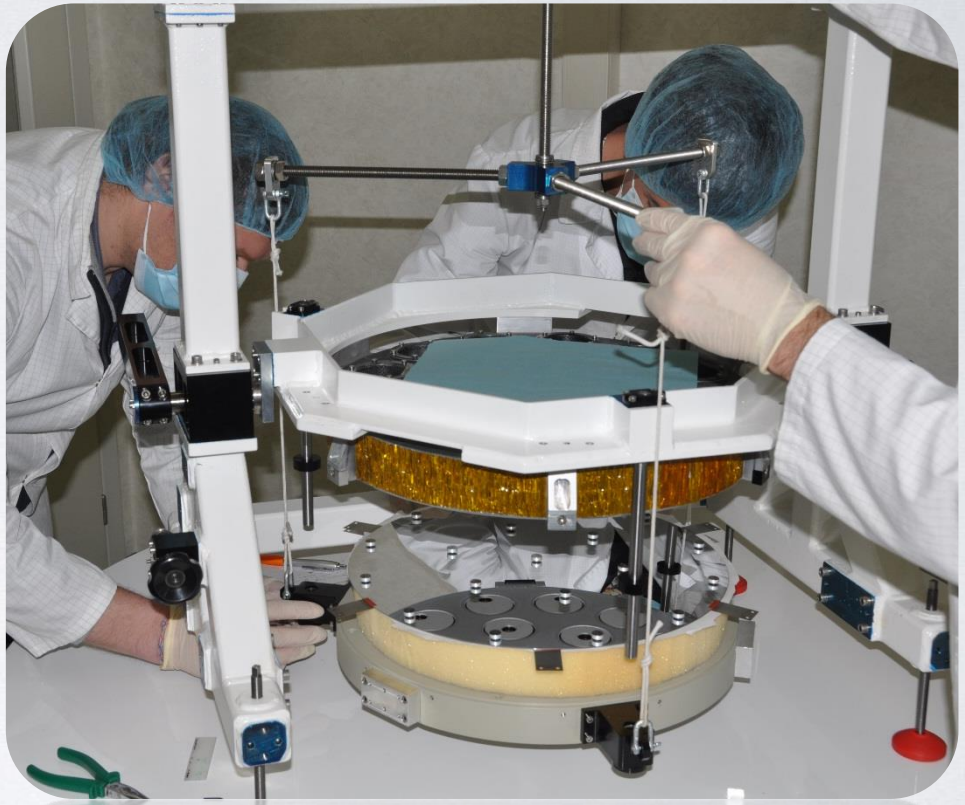
Gait Analysis for medical rehabilitation and injury prevention

MPD
MICRO PHOTON DEVICES

Single photon counting modules based on SPAD technology

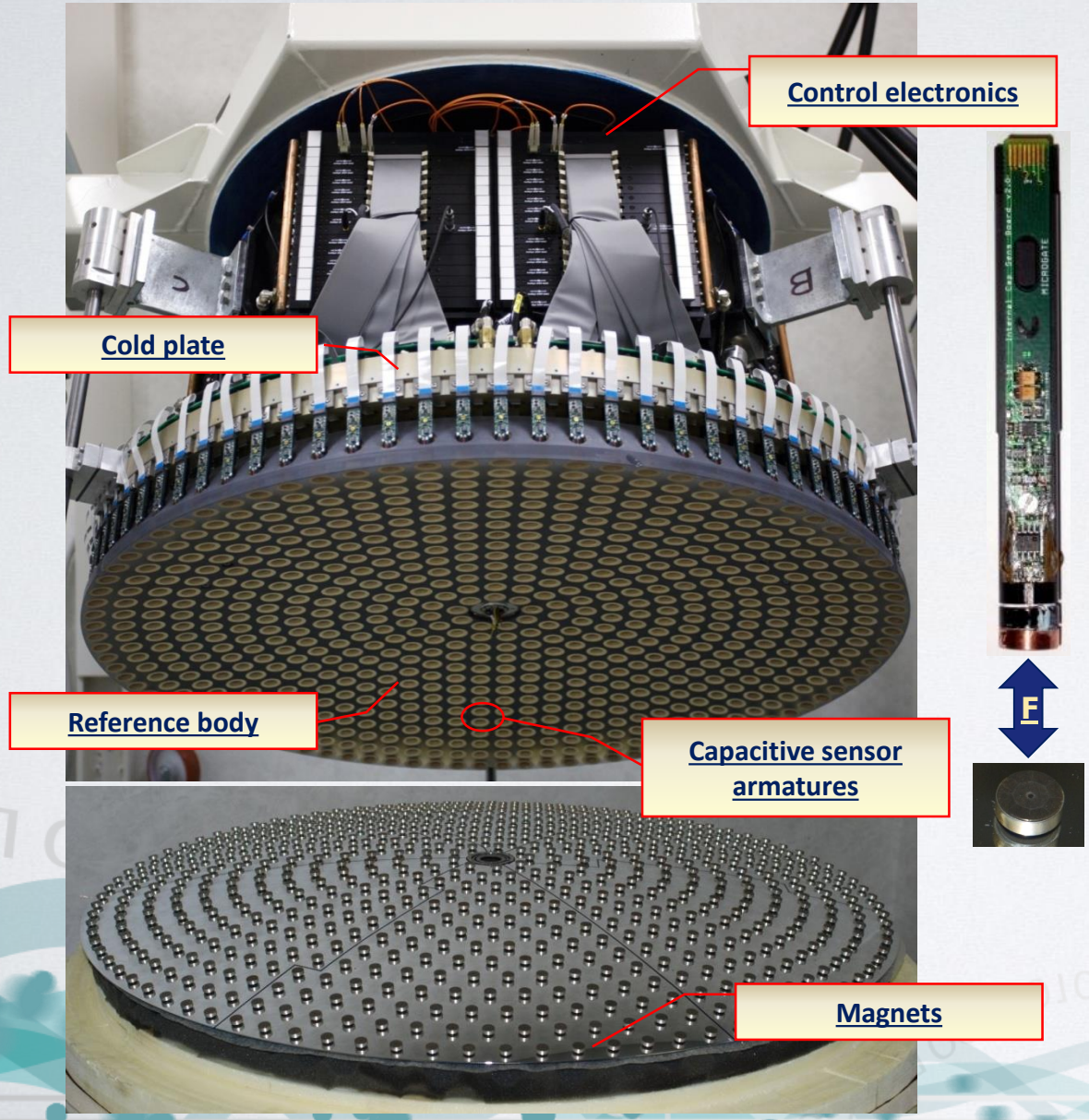
Capabilities

- **42+ employees**: 15 engineers with 5 PhDs among them (4 aerospace, 7 electronics, 4 computer science)
- The internal capabilities cover the entire process of **electronic systems design and manufacturing**
  - Hardware design (digital, analog)
  - Firmware (FPGA, microcontrollers)
  - Software
  - Control system design and multiphysics simulation
  - Prototyping
  - Integration of complex mechatronics systems
  - Testing
  - Production



MICROGATE

Background: *large, contactless adaptive mirrors*

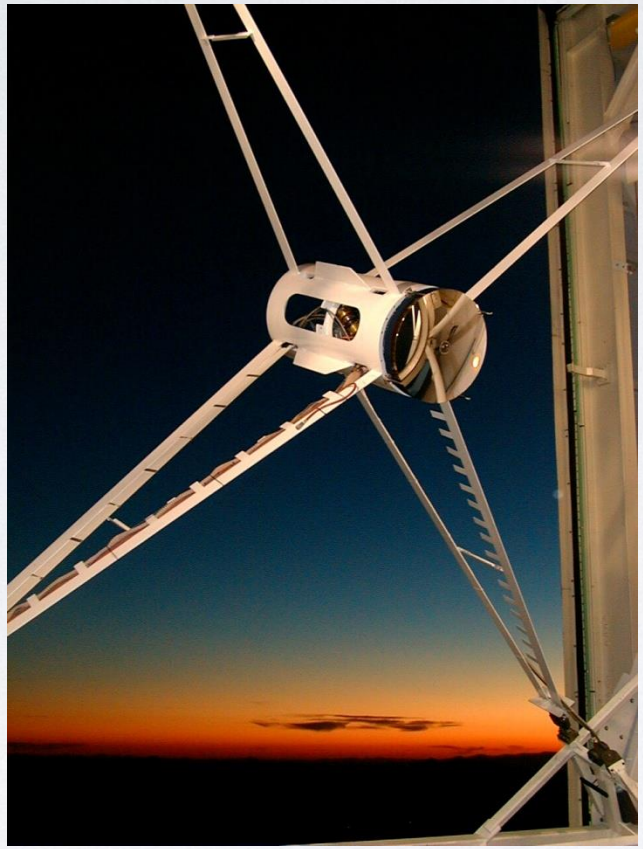


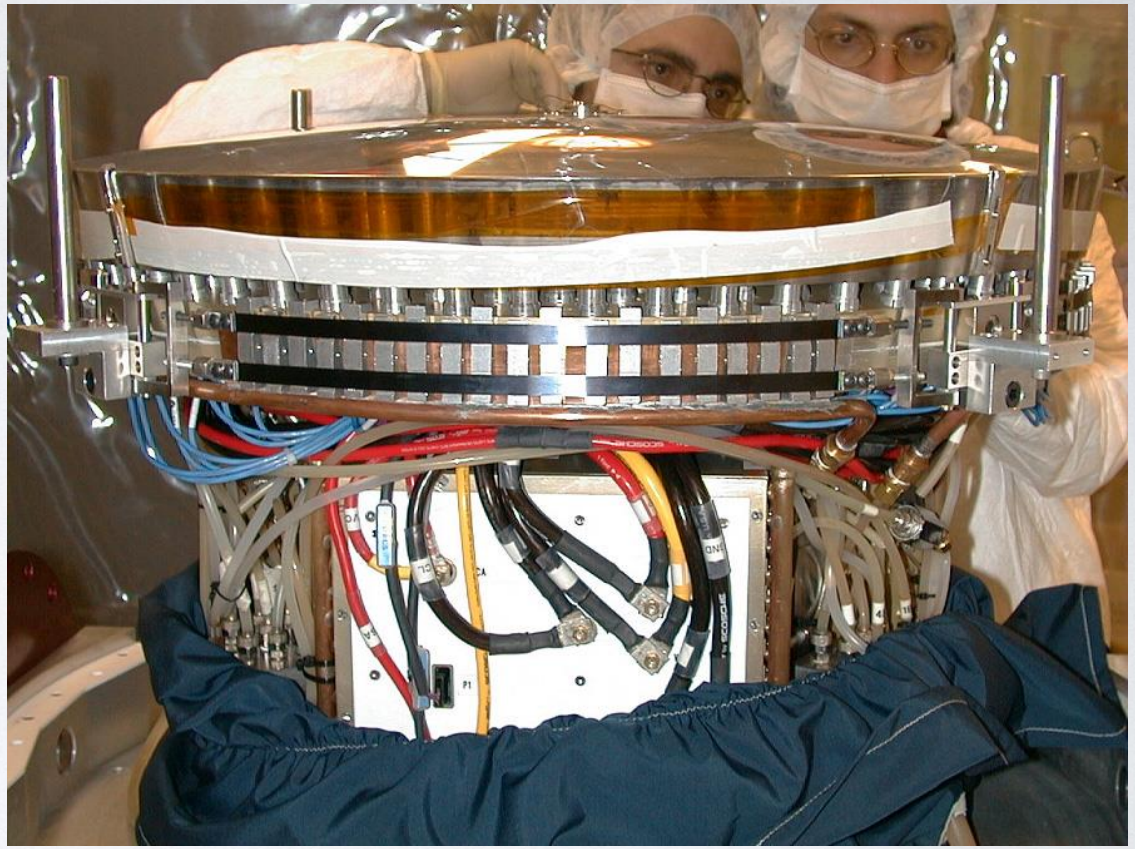
- The thin (< 2mm) mirror **levitates** and is actively and massively controlled by a **large number (336 … > 5000)** of electromagnetic **actuators**
- The actuators are **contactless**, only magnetic forces are transferred to the mirror
- The distance feedback is provided by co-located **capacitive sensors** measuring the distance between thin mirror and reference surface
- Positioning accuracy: 3nm
- Settling time: 0.7ms
- **Co-located control ~80kHz**, > 5000 channels
- **Global control** up to 2kHz involving several large **MVMs** (up n > 5000) to be executed in **< 200µs**
- **On-board electronics** (signal integrity, harness)

MICROGATE

MMT336

- MMT336 is the first adaptive secondary mirror ever built
- 0.64m shell diameter, 336 actuators
- Operational since 2002 on the Multiple Mirror Telescope, Mt.Hopkins, AZ
- Cluster of **168 ADSP-2181 16 bit integer DSPs**
- Altera CPLD (communication, glue logic)

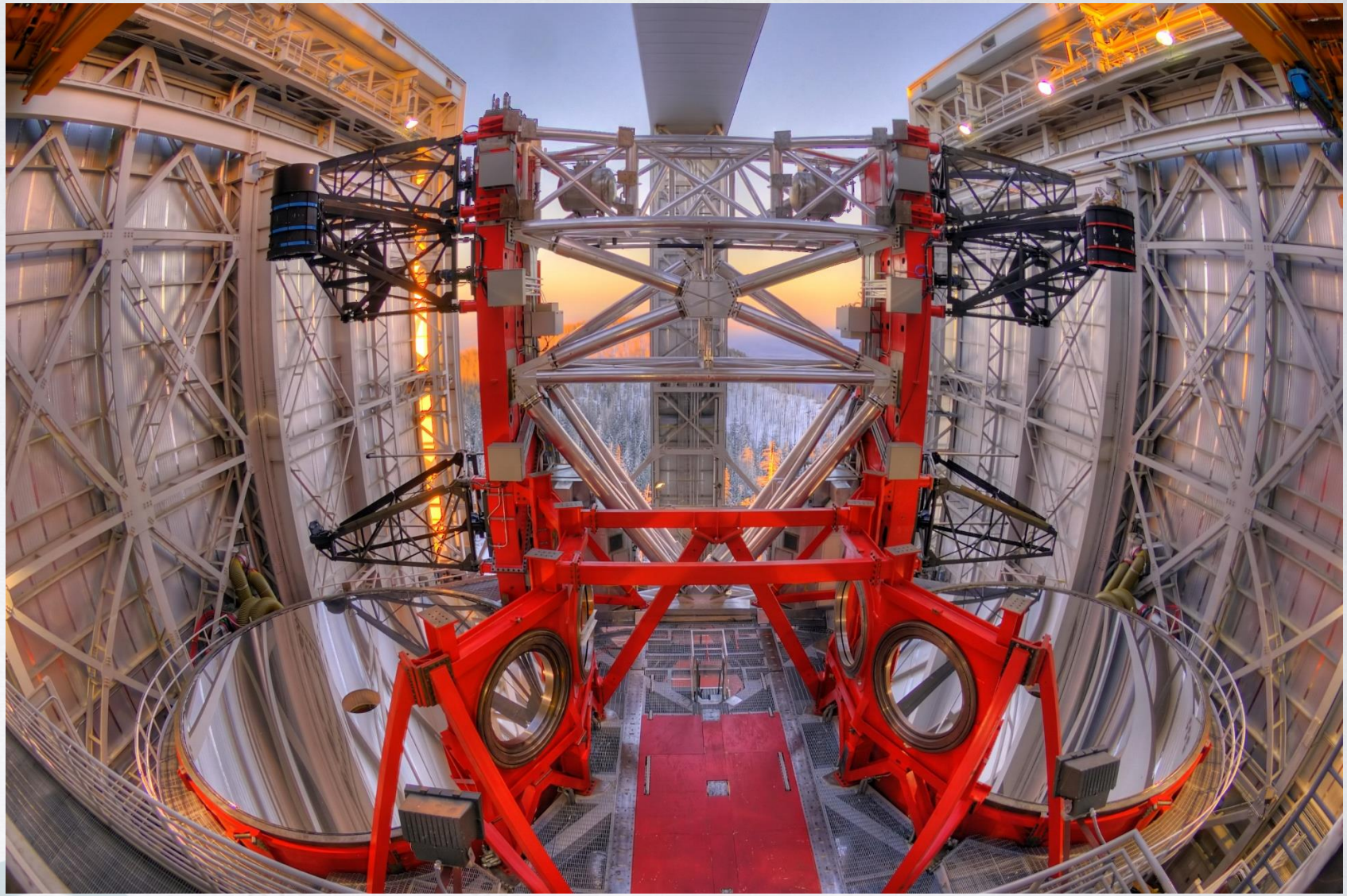




MICROGATE

LBT672 (2 units) + Magellan

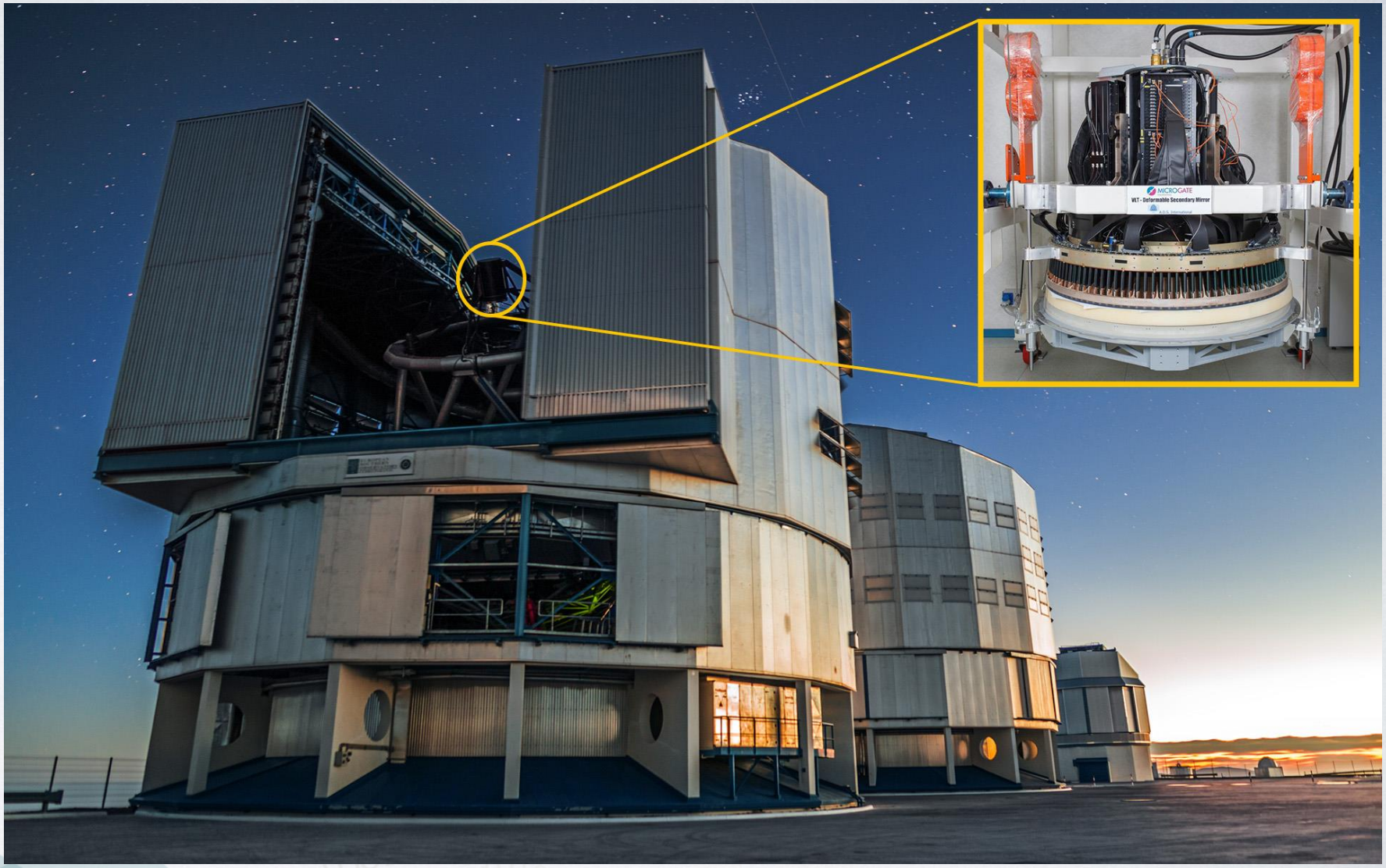
- Large Binocular Telescope
  - 2x8.4m primary
  - Mt.Graham – Arizona
  - Two adaptive mirrors, 0.91m shell diameter, **672 actuators**
- Magellan Baade
  - 6.5m primary
  - Las Campanas, Chile
  - 0.85m shell diameter, **585 actuators**
- Cluster of **168 ADSP-TS101 FP32 DSPs** (0.5 GMAC/s each, 84 GMAC/s total)
- **~2004 design**
  at the telescope starting from **2008**
- Altera Stratix 1 (communication, glue logic)
- **On-board RTR** + external slope computer based on same technology
- Zero slope computation latency with Pyramid (and SH),
  ~200µs overall latency
- Recently upgraded to 2kHz operation and CameraLink interface to OCAM2 (SOUL + MAG2k)



MICROGATE

VLT DSM

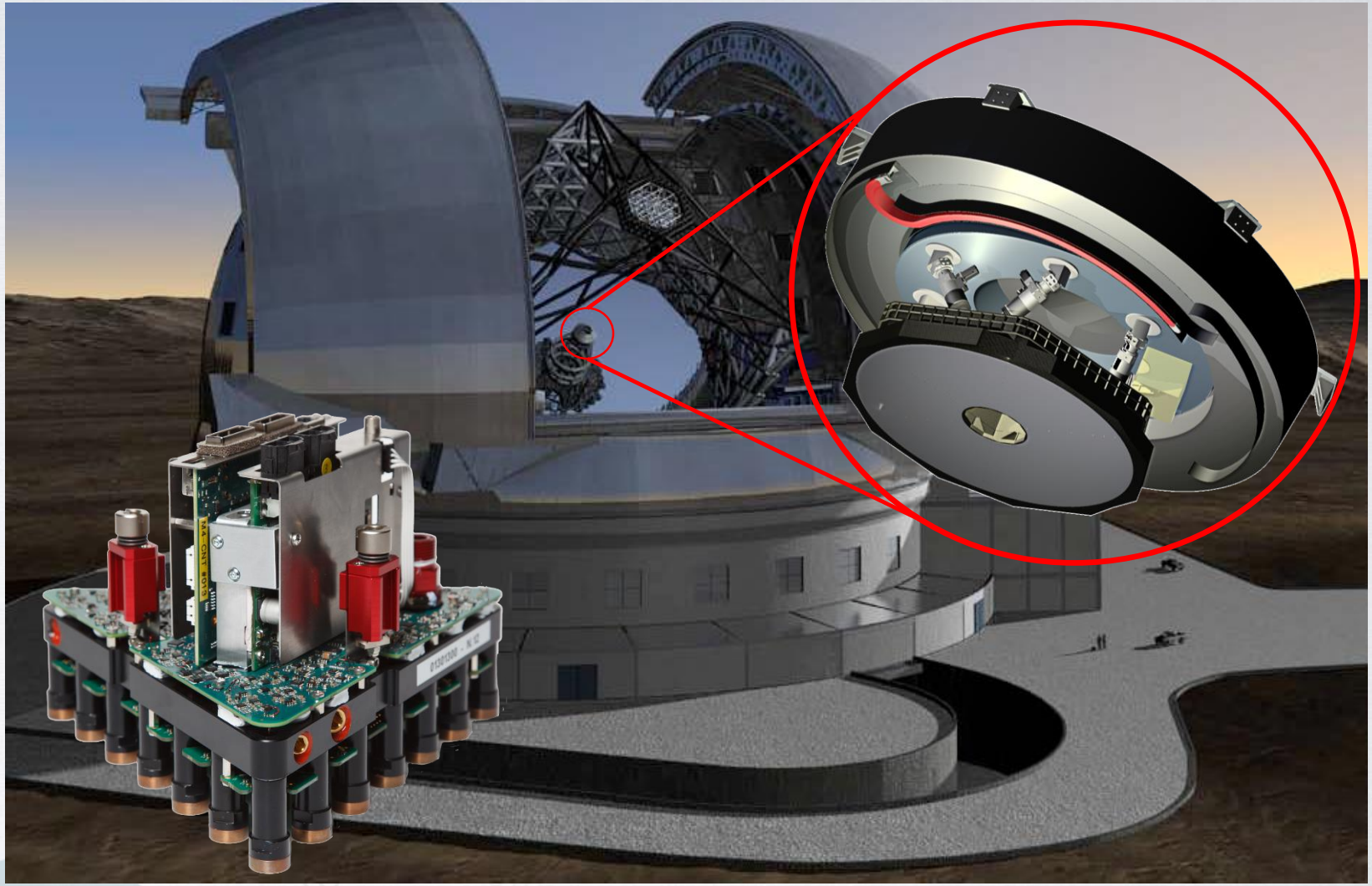
- Very Large Telescope (ESO, Paranal, Chile)
- four 8.2m telescopes
- the largest Adaptive Mirror ever built: 1.12m diameter, **1170 actuators**
- Cluster of **156 ADSP-TS201 FP32 DSPs** (1 GMAC/s each, 156 GMAC/s total)
- **~2007 design** at the telescope since **2016**
- Altera Stratix 2 (communication, glue logic)



MICROGATE

ELTs

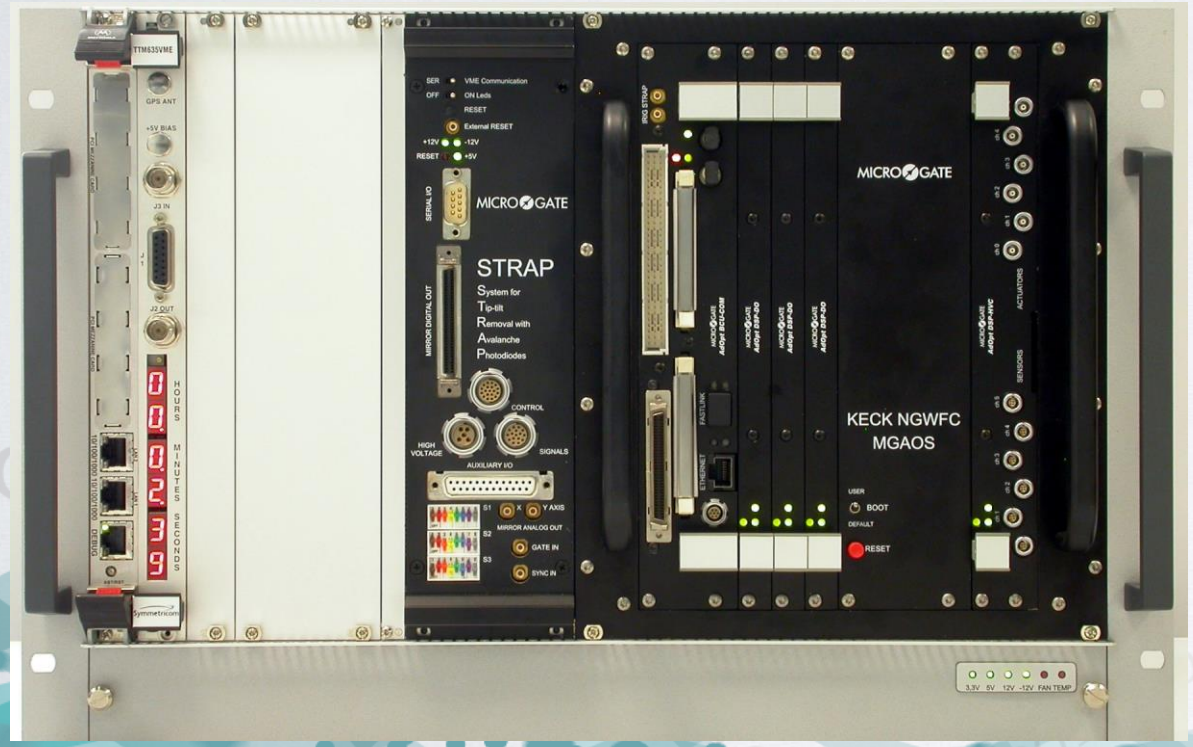
- **ESO E-ELT**
  - Cerro Armazones (Chile)
  - Primary mirror: 39m
  - 39m primary, adaptive M4, 6x segmented, 2.5m diameter
  - **6x892 = 5352 actuators**
  - FDR passed, now in construction, acceptance 2024
- **GMT**
  - Cerro Las Campanas (Chile)
  - 7x8.4m primary, 7x1.05m adaptive secondary
  - **7x672 = 4704 actuators**
  - Electronics FDR passed
- Cluster of **~180 ARRIA V FPGAs** (1045 FP DSP blocks)
  - 0.5 TMAC/s for global control MVM
  - local control, communication, …
- **µXLink board**



MICROGATE

Background: Keck NGWFC

- The current Keck RTC (New Generation Wavefront Controller) has been developed and produced by Microgate
- CFT 2004, delivery June 2006
- Based on Microgate proprietary DSP boards (developed for large contactless adaptive mirror control – LBT, Magellan) + VME embedded computer



- Still very performant SCAO system
  - **CCD39** (+ CCDi56, never deployed) for **NGS and LGS WFS**
  - **STRAP** (Microgate product) + **TRICK** based on HRG2 CCD for **multiple ROI TT sensing**
  - Mirrors: **Xinetics DM** with 349 actuators + **down TT** + **up TT**
  - Large telemetry storage (Telemetry Recorder Server), 5.6TB, 5 nights, Postgres
  - Very low latency
- High reliability

MICROGATE

Background: GreenFlash

- H2020 project, started end 2015, **completion end 2018**
- Goal: Energy efficient high performance computing for real-time science
  - Real-time HPC using accelerators and smart interconnects
  - Energy efficient platform based on FPGA for HPC
  - AO RTC prototyping and performance assessment
- Partners:

l'Observatoire de Paris — LESIA
Laboratoire d'Études Spatiales et d'Instrumentation en Astrophysique

Project leader (Damien Gratadour); GPU technology

Durham University

CPU technology

MICROGATE ENGINEERING

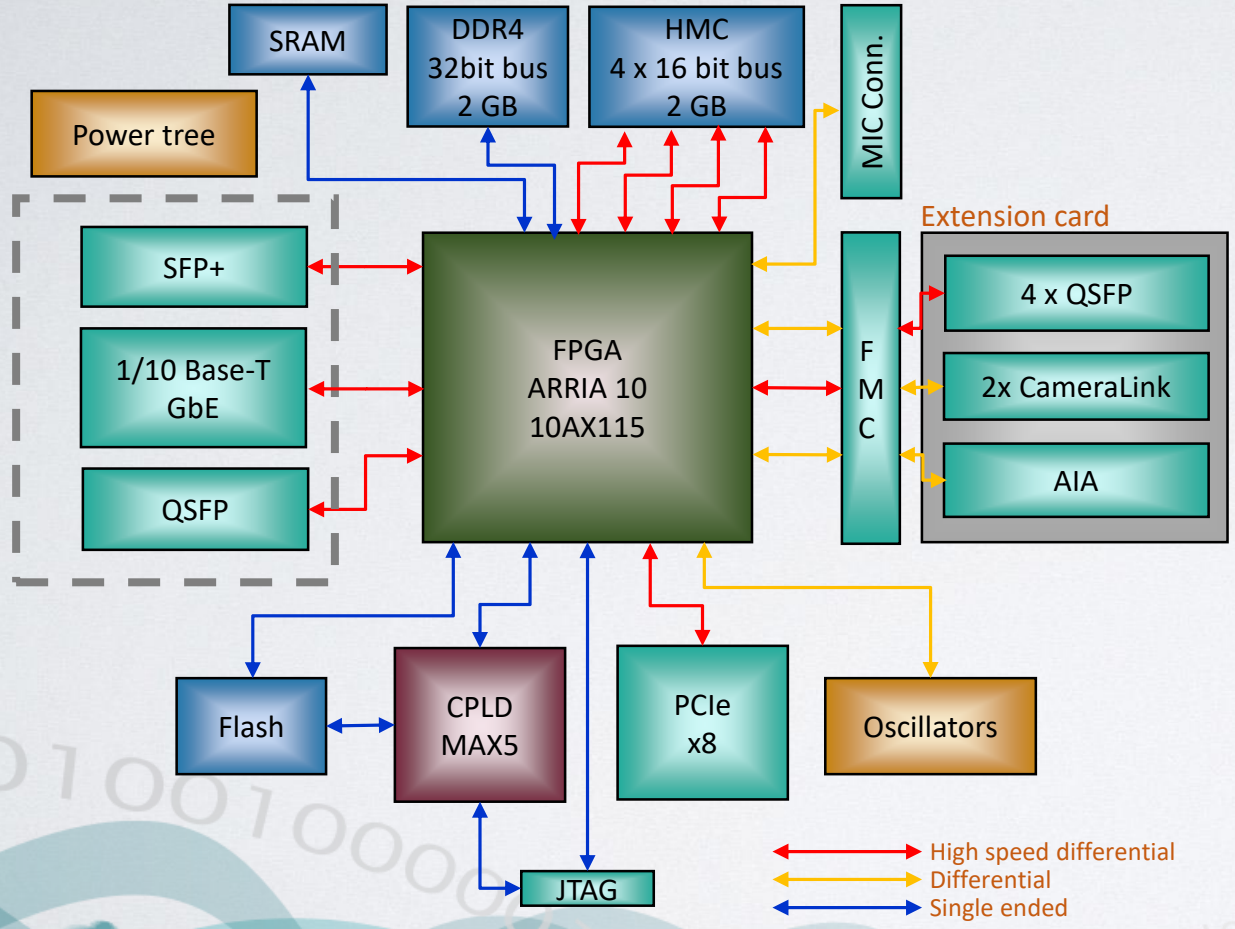
FPGA technology

Accelize®

Smart Software tool for FPGA programming (QuickPlay)

Background: GreenFlash – Microgate µXComp board

Designed for heavy computational tasks



Designed for heavy computational applications

Board features:

- Based on the Intel ARRIA 10AX115
- Max. nr. Transceivers -> 96 (used 95)
- 1518 DSP blocks
- 5.3MB FPGA internal RAM
- MAX V board controller for programming and housekeeping
- PLL chip with 8 differential and 4 single-ended outputs to program variable refclks for different interface standards
- 1Gb NOR Flash
- 2 GB DDR4
- **2 GB HMC memory with 4 links (64 transceivers) - 88.7GB/s** demonstrated (22 GMAC/s sustained MVM)
- PCIe endpoint with Gen3 x8 edge connector

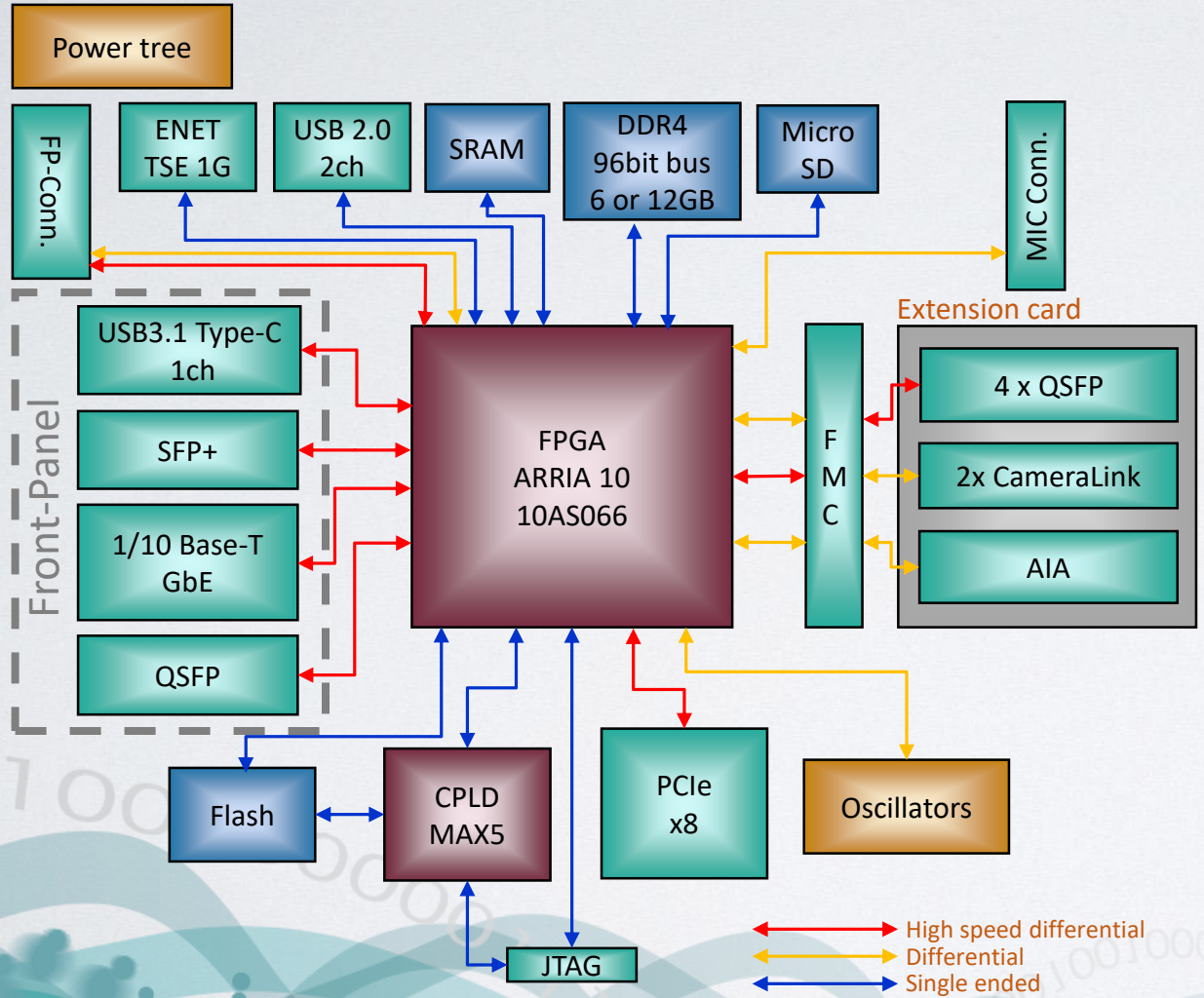
On-board interfaces:

- 8 lanes PCIe up to Gen3 for endpoint
- SFP+ for 10GbE (or different interfaces)
- RJ-45 for 1G/10G Ethernet over copper
- QSFP for 40 GbE or Infiniband (or different interfaces)
- Configurable digital I/O connector , e.g. to handle synchronization signals (MIC Connector)
- FMC connector

MICROGATE

Background: GreenFlash – Microgate µXLink board

Designed for smart interfacing and host-less applications



Board features:

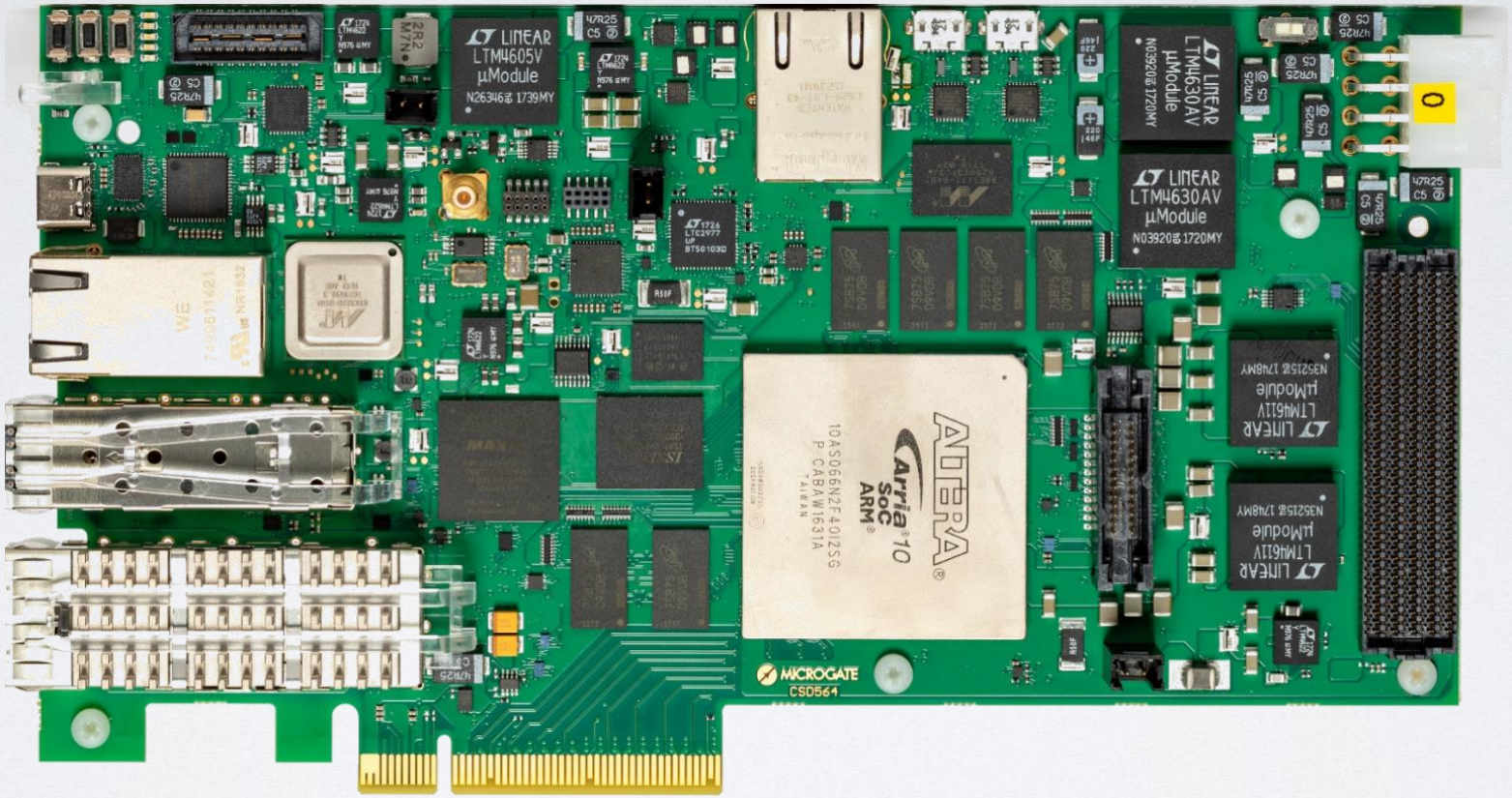
- Based on the Intel ARRIA 10AS066 SoC
- Dual core **ARM Cortex-A9 embedded processor** (with OS)
- Max. nr. Transceivers -> 48 (used 43)
- 1855 DSP blocks
- 5.2MB FPGA internal RAM
- 6 GB DDR4 (no HMC because only 48 transceivers)
- Can be configured as well as **powerful PCIe root complex** because of ARM and OS (e.g. Linux) for a stand-alone box

On-board interfaces:

- 8 lanes PCIe up to Gen3 as endpoint or root
- SFP+ for 1G/10GbE (or different interfaces)
- RJ-45 for 1G/10G Ethernet over copper
- QSFP for 40 GbE or Infiniband (or different interfaces)
- USB3.1 Gen 2 Type-C to connect external hard drives, monitors, docking stations
- 2x USB2.0 directly to ARM co-processor
- 1G Ethernet directly to ARM co-processor
- MicroSD card slot directly to ARM co-processor
- Configurable digital I/O connector , e.g. to handle synchronization signals (MIC Connector)
- FP-Connector to attach a second front-panel
- FMC connector equal to µXComp for expansion boards on which several additional interfaces can be implemented, e.g. other 10GbE, CameraLink, S-FPDP, …

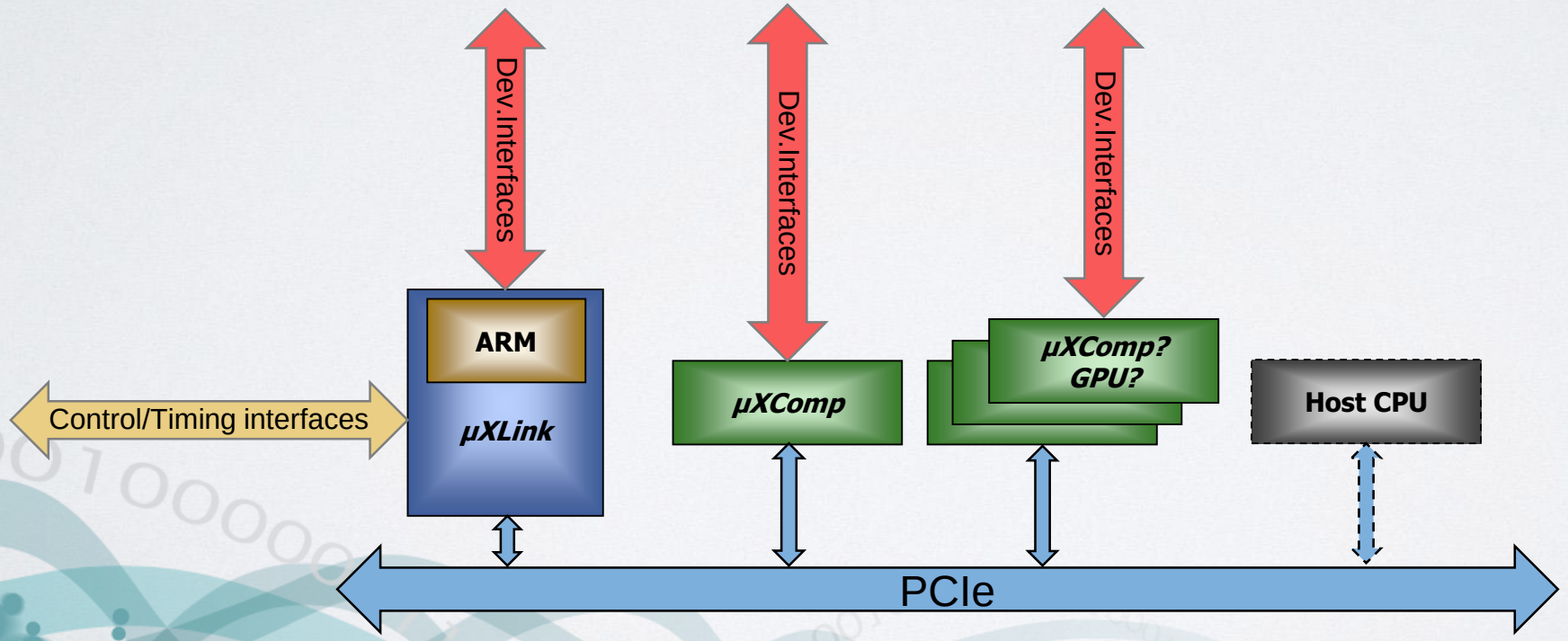
MICROGATE

Background: GreenFlash – Microgate µXLink board



Background: GreenFlash – MicroServer concept

Our implementation of the Microserver concept comprises a PCIe backplane, on which the FPGA-based board µXLink that provides most of the interfaces the ARM co-processor with a OS and features PCIe root complex capability. In this way, the Microserver can operate in **standalone mode**, without requiring an additional host CPU. Several µXComp or GPUs can be inserted in the PCIe backplane and communicate with the µXLink. This allows achieving **optimal energy efficiency, low data transfer latency, low jitter and efficient management of telemetry data**.



MICROGATE

Keck RTC RFP

- **RFP** for a new RTC system for Keck I and II issued in **December 2017** – competitive tender
- **Microgate** and Damien Gratadour decided to respond jointly to the Keck CFT, involving also **Swinburne University** and **Australian National University**
- Proposal selected out of three (?) bidders
- Team:
  - Microgate - team leader
  - Swinburne University - nominated subcontractor (Damien Gratadour joining in few weeks from now)
  - Australia National University (François Rigaut) supporting Swinburne
- Contract signed in April 2018
- **Project schedule:**
  - PDR: December 2018
  - DDR: May 2019
  - Pre-shipment acceptance: May 2020 (first system)
  - Post-delivery acceptance: July 2020
  - 3 system delivered to Keck by 2020
  - **First light in late 2020**

MICROGATE

Keck RTC: requirements

***Just* a 10m telescope, but quite ambitious…**

- **11 different operating modes**, combining different WFSs and mirrors, NGS, LGS
- **3** operating **modes** comprehend **Laser Tomography AO** (not part of 2020 deliverables)
- **Telemetry**: **10 nights** decimated (100 Hz) + 10x 1min/hour full speed
- Maximum WFS updated rate (control cycle): **2kHz**, but scalable to 4kHz with **250µs latency**

MICROGATE

Keck RTC: requirements - interfaces

- **legacy NGWFC sensors**
  - **CCD39** with **AIA** interface (40x40 SH WFS)
  - Microgate **STRAP** with **RS422** interface -formerly VME (TT)
  - **TRICK** based on HRG2 CCD with **HotLink** interface – recently added to the existing NGWFC (multiple ROI NIR TT sensing, up to 8 ROIs, up to 16x16 pixel subaperture)
- **new sensors**
  - **OCAM2** with **CameraLink** interface (40x40 SH WFS)
  - **UoH Saphira** with **USB3.1** interface (80x80 PWS)
  - **E2V CCD 4270** with **CameraLink** interface (2k x 2k acquisition camera)
- **legacy NGWFC mirrors**
  - **Xinetics DM** with FPDP parallel interface (349 actuators)
  - Up Tip-Tilt mirror directly controlled by Microgate HVC piezo-controller
  - Down Tip-Tilt mirror directly controlled by Microgate HVC piezo-controller
- **new mirrors**
  - **Boston Micromachines MEMS** with Aurora 2.5Gbit/s fiber interface (952 actuators)
  - Additional 3x Down Tip-Tilt mirror directly controlled by Microgate HVC piezo-controller
- **Telescope control system**
  - Evolution of existing Wavefront Controller Interface
  - PTP for timing reference

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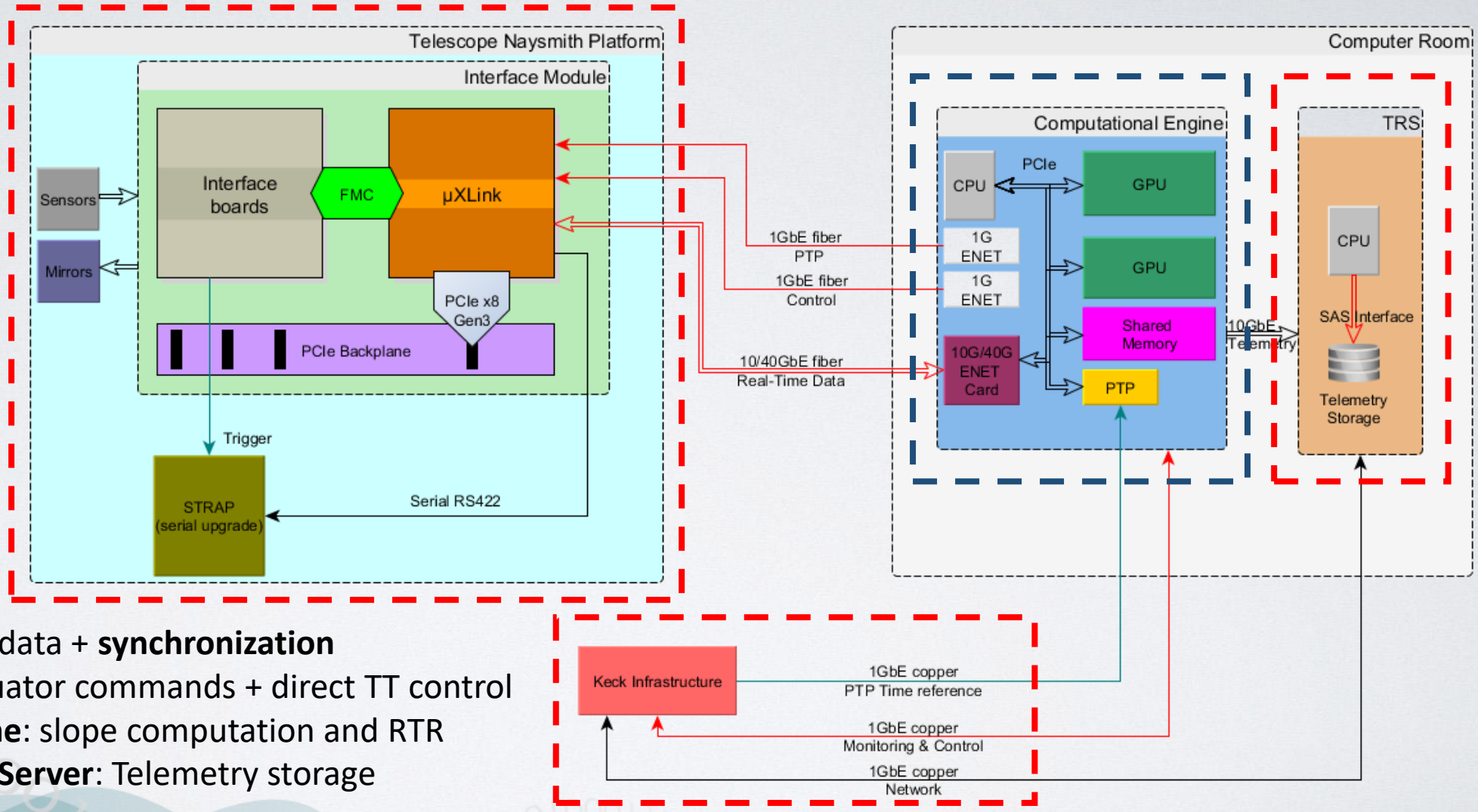
Keck RTC architecture

Microgate

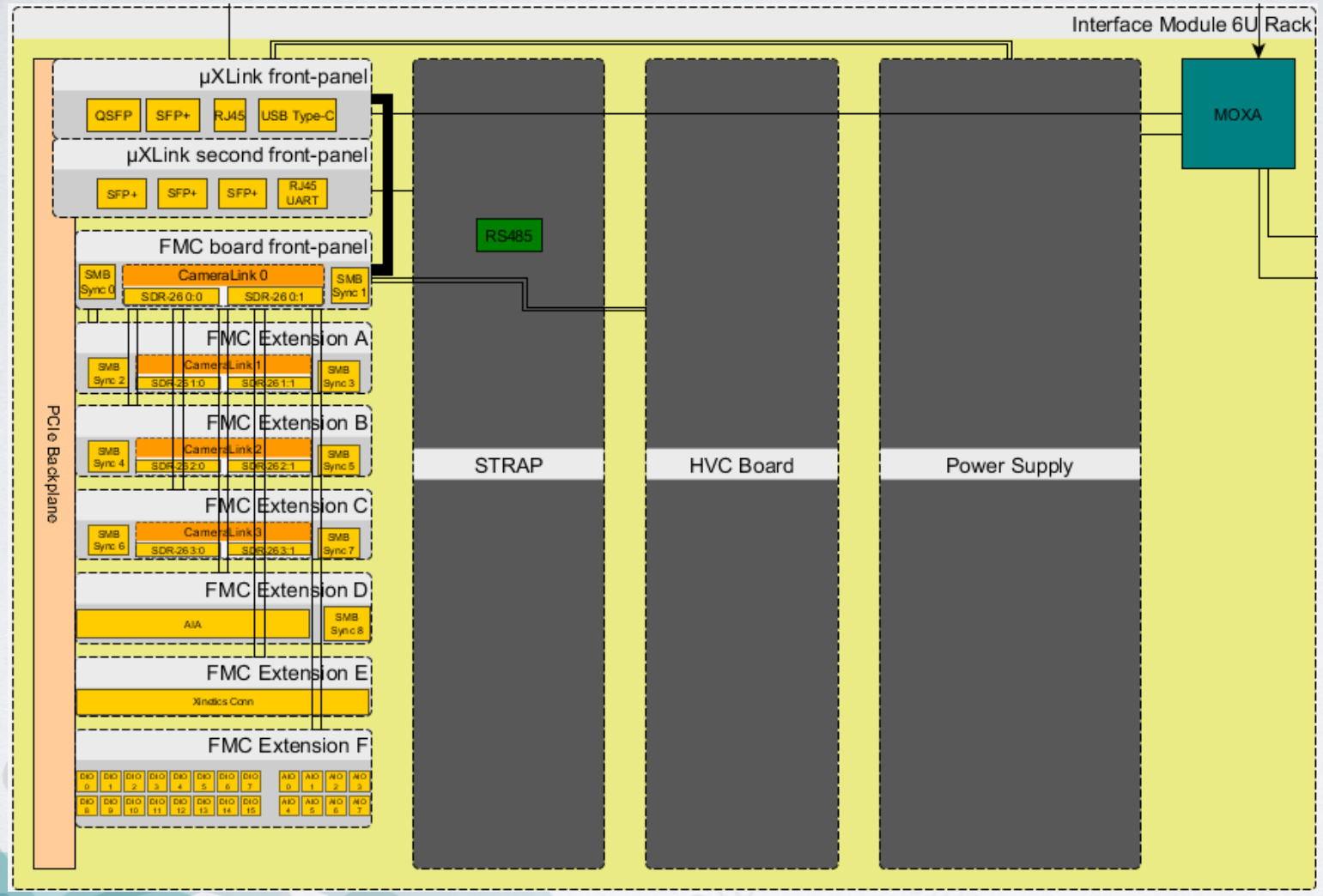
SUT/ANU



- **Interface module**
  - Merging sensor data + **synchronization**
  - Distributing actuator commands + direct TT control
- **Computational engine**: slope computation and RTR
- **Telemetry Recorder/Server**: Telemetry storage

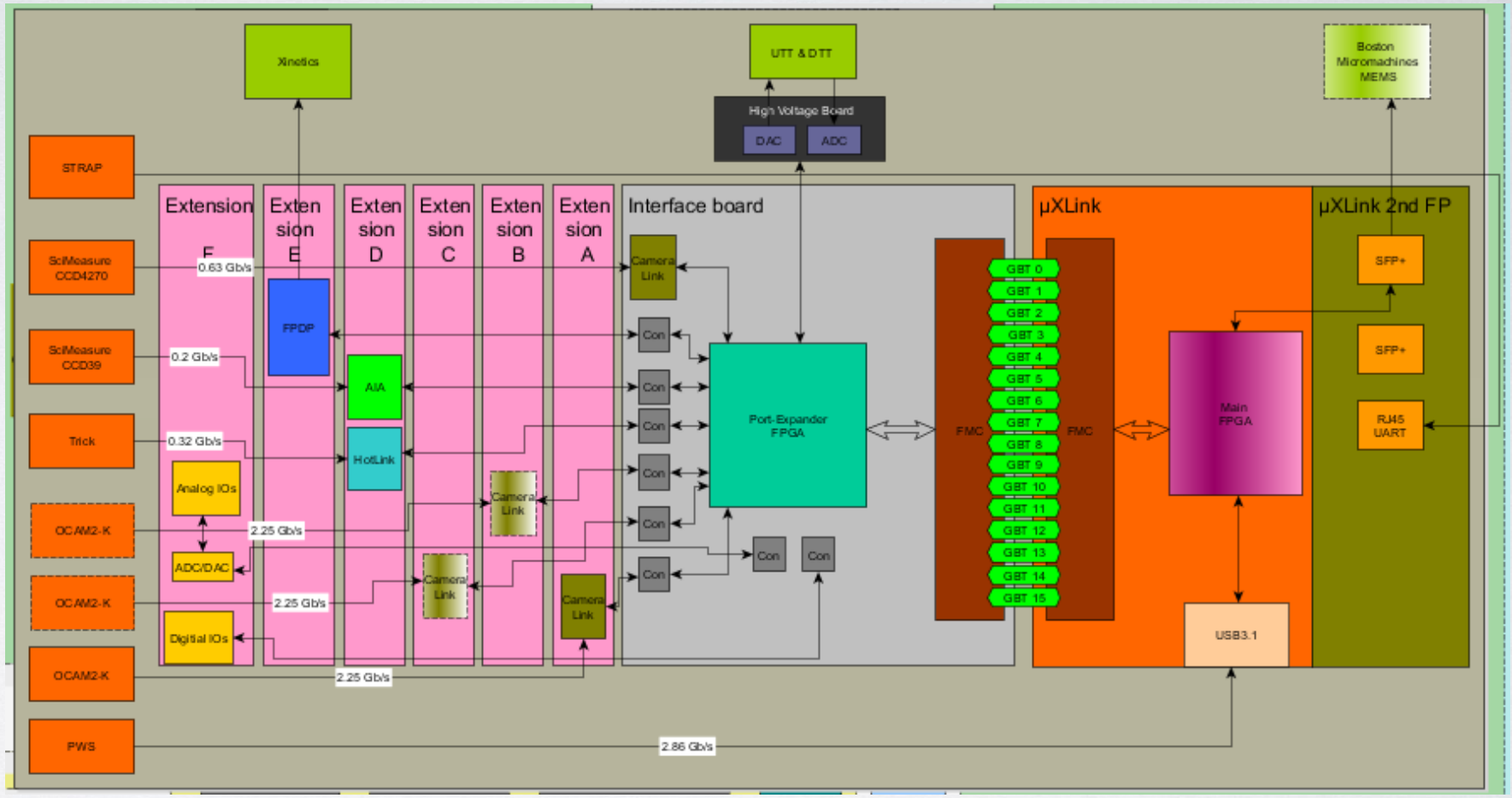
MICROGATE

Interface Module



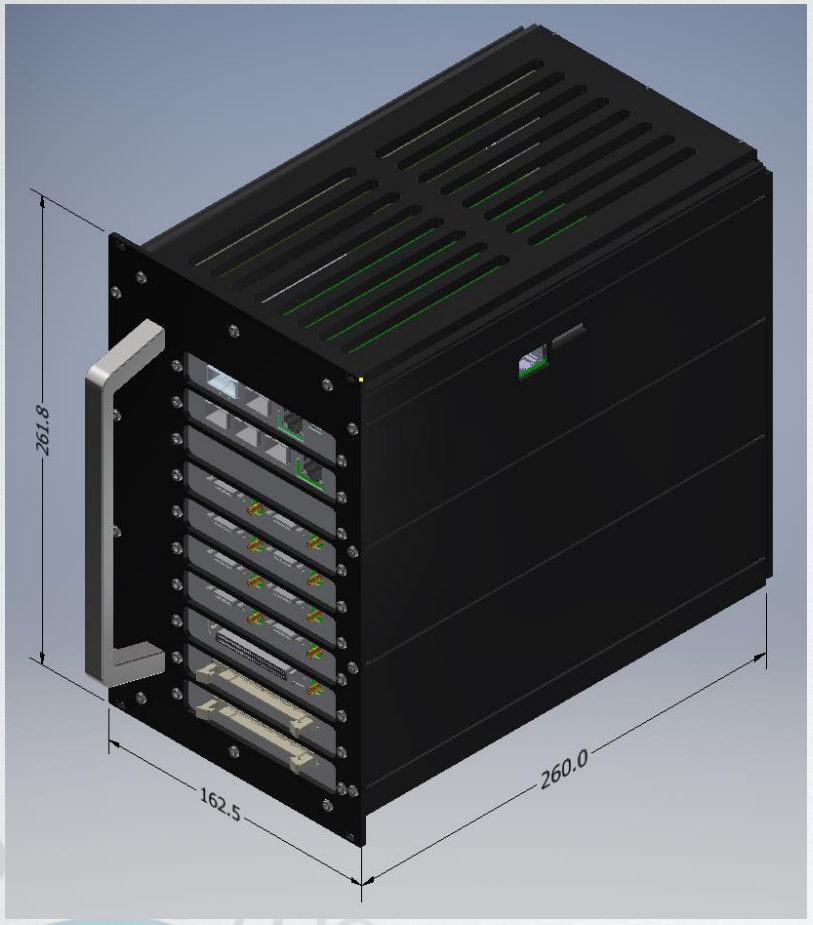
Interface module block diagram

- **µXLink** is the core of the Interface module
- **Additional interface board** connected to the **FMC** interface for flexible interfacing to sensors and actuators
- Simple passive **Extensions boards** to provide the physical interfaces
- **µXLink** installed on a PCIe backplane, acting as PCIe root. **Not used** in the baseline design, but ready for further expansion



MICROGATE

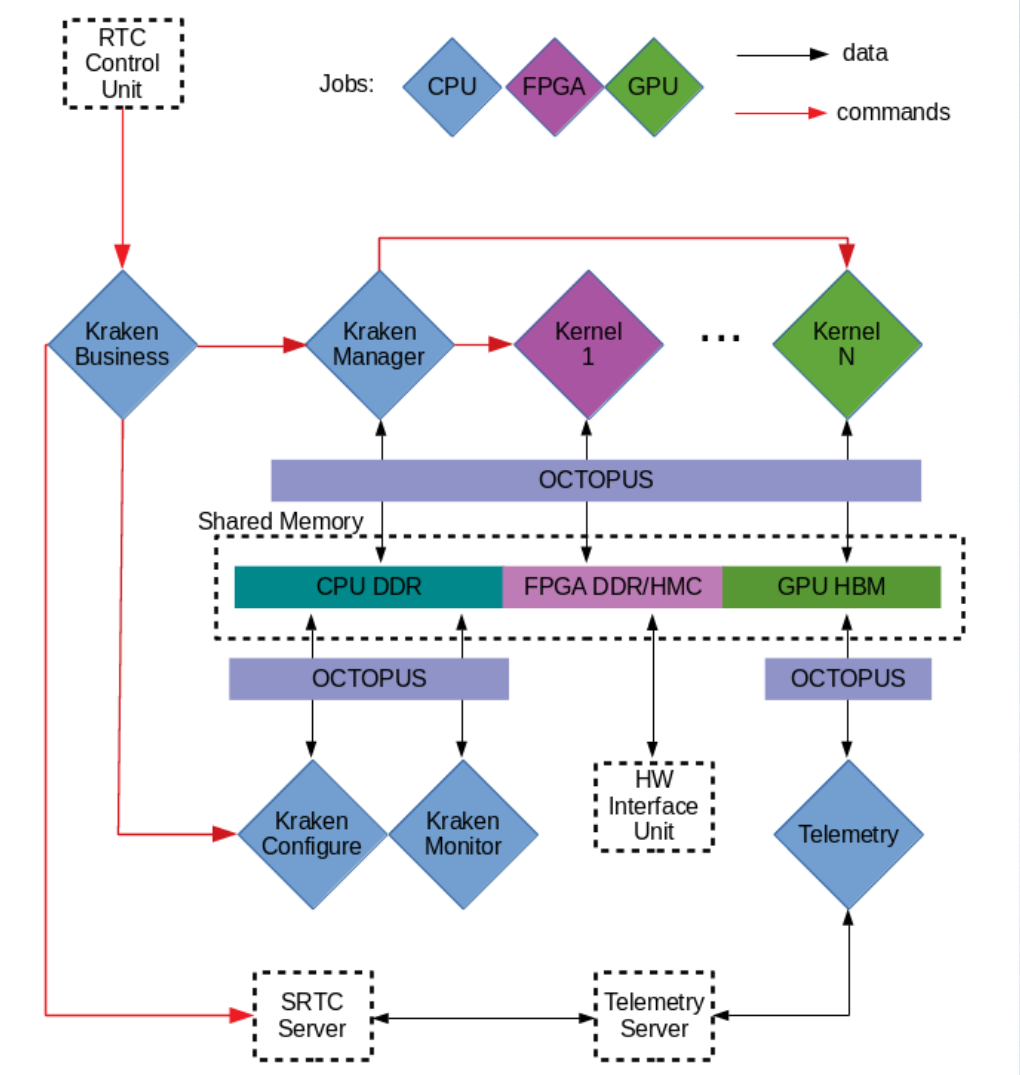
Keck RTC Interface Module



Keck RTC Computational Engine

Computational engine architecture

- Based on Nvidia 2x V100 GPU, one dedicated to the real-time pipeline, the other so simulation
- Software standardization: first deployment of COSMIC project
- Unified SHM concept through Octopus
- Each job is assigned its own specialized Interface depending on RTC system Configuration
- Kraken manager starts jobs and performs housekeeping (jobs + memory)
- Kraken business is the sequencer
  - starts manager, configure and monitor
  - direct interface with other subsystems



MICROGATE

Keck RTC Telemetry server

Telemetry recorder/server architecture and preliminary dimensioning

- Based on N1x Single 8Gbit FC RAID Controller – with 12 bays + 12 bays expansion
- 24x Hot-Swap 4TB, 7200RPM, 6Gbit SAS Disk Drive w/ Carrier

  Magnetic disks selected vs. SSD to reduce cost. Need qualification for elevation
- 8Gbit Single Port Fibre Channel Card (HBA) – Qlogic
- RAID 6 configuration
- Postgres used for database management
- From preliminary evaluation, the TRS task requires 2 CPUs of the host machine. As baseline, will run on a separate machine to avoid bus contention issues

MICROGATE

Conclusions

- First tangible **outcome of the GreenFlash** project
- **Modular, expandable** system
- Exploits **flexibility of FPGAs** for **interfacing**, data merging, synchronization and throughput of **GPUs** for the **bulky computation**
- Full **simulation** capabilities included in the design
- Attempt to **standardize** the **software** platform - COSMIC
- Tailored to current 8-10m class telescope, but **concept expandable to ELTs**
- Implementation timescale suitable to be a **precursor of ELTs systems**

MICROGATE