A Scalable Platform for Adaptive optics Real-time Control on FPGA

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From small telescopes to ExAO

AO on small telescopes

• Plug-and-play AO (simple architecture) with off-the-shelf development boards.

• Compatibility with Arduino shields (standardization) with higher FLOPS/chip area compared to MCUs.

• Inexpensive and portable, with standard interfaces.

Extreme-AO

• Extremely low jitter and latency requirements.

• Large MVM and memory bandwidth.

<table>
<thead>
<tr>
<th>Status</th>
<th>DM&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Primary WFS(s)&lt;sup&gt;b&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Palm3000+P1640, Palomar (5 m)</td>
<td>Operation 2012–2017</td>
<td>66</td>
</tr>
<tr>
<td>GPI, Gemini (8.2 m)</td>
<td>Operation 2014–present</td>
<td>50</td>
</tr>
<tr>
<td>SPHERE, VLT (8.2 m)</td>
<td>Operation 2014–present</td>
<td>50</td>
</tr>
<tr>
<td>SCExAO, Subaru (8.3 m)</td>
<td>Operation + development</td>
<td>48</td>
</tr>
<tr>
<td>MagAO-X, Magellan (6.5 m)</td>
<td>Development</td>
<td>48</td>
</tr>
</tbody>
</table>

Courtesy: Guyon (2018)
Scalability

Targets
• Number of subapertures and pixels per subaperture
• Memory bandwidth (DDR-scalable, HBM/HMC in future).
• Interoperable with Xilinx FPGAs

Challenges
• Programming Overhead
• Backward Compatibility

Implementation
• Xilinx VC-709 with Virtex-7 690T and 2x4GB DDR3 (12.8 GB/s peak per chip)
• Before HMC and HBM2
**Dataflow**

- **WPU** – Acquire pixels from CCD interface, and scalable slope computer (clk_pixel and clk_slope). Flexible BRAM addressing and modular slope computation.

- **AO Reconstructor** – Adapts to the memory speed (of the reconstruction matrix) and computes the DM outputs from WF slopes, by instantiating the required number of DSPs. Scalability of subapertures and memory speed implemented here.

- **Memory state machine** – Creates buffer between AO reconstructor and external memory. Intermediate FIFO can adapt to different datawidth and clock frequency of external memory.
Scalability

**Diagram Description:**
- **Scalability**
  - **Bank A** Memory Interface Generator
  - **Bank B** Memory Interface Generator
  - **Reconstructor FIFO A**
  - **Reconstructor FIFO B**
  - **Reconstruction Matrix**
  - **X-slope**
  - **Y-slope**
  - **Intermediate phase (nrow, ncol)**
  - **Intermediate phase (nrow, ncol - 1)**
  - **Intermediate phase (nrow, ncol + n²)**

**Legend:**
- **Clock frequency**
- **Clock**
- **Data width**
- **Data Bus**
• Scalability before synthesis, needs to be routed after scaling.

• 512 DSPs per clock cycle for current DDR3. 3,600 DSPs available in 690T.

• Kernel determines RAM vs availability of DSPs and optimizes for maximum performance.

\[
recon_{\text{clk}} = \frac{d\text{dr}_{\text{clk}}}{nCK \times nfifo}
\]

\[
f fifo = \frac{d\text{dr}_{\text{clk}}}{nCK \times recon_{\text{clk}}}
\]
HIL Simulation and iRobo-AO loop

Table 1: AO correction at different subaperture sizes and telescope aperture diameters. The input wavefront is simulated with a Fried parameter ($r_0$) of 15 cm, a mean wind velocity ($v$) of 5 m/s and an outer scale of turbulence ($L_o$) of 25 m.

<table>
<thead>
<tr>
<th>Subapertures</th>
<th>Aperture Diameter (in meters)</th>
<th>Mean RMS WFE (in radians)</th>
<th>Fitting + Time Delay error</th>
<th>Strehl Ratio</th>
<th>Factor of Improvement in RMS WFE</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 x 50</td>
<td>8</td>
<td>9.03</td>
<td>0.54</td>
<td>0.62</td>
<td>0.75</td>
</tr>
<tr>
<td>42 x 42</td>
<td>6</td>
<td>5.10</td>
<td>0.43</td>
<td>0.57</td>
<td>0.83</td>
</tr>
<tr>
<td>32 x 32</td>
<td>5</td>
<td>3.44</td>
<td>0.33</td>
<td>0.60</td>
<td>0.90</td>
</tr>
<tr>
<td>21 x 21</td>
<td>4</td>
<td>2.18</td>
<td>0.24</td>
<td>0.70</td>
<td>0.94</td>
</tr>
<tr>
<td>16 x 16</td>
<td>3</td>
<td>1.49</td>
<td>0.27</td>
<td>0.68</td>
<td>0.93</td>
</tr>
<tr>
<td>11 x 11</td>
<td>2</td>
<td>0.99</td>
<td>0.20</td>
<td>0.65</td>
<td>0.96</td>
</tr>
</tbody>
</table>
Resources, Memory and Time
Summary

- Median time of 1.283 ms from availability of first WFS pixel at the FPGA to the last actuator value exit at the PCIe interface.
- Real time AO reconstruction performance of 21.4 GFlops for an external memory bandwidth of 21.4 GB/s (16-bit fixed-point).
- FPGA resource usage of less than 30 %.
- FIFO buffer allows for the isolation of external memory enabling automatic adjustment of memory modules of different clock frequencies and data-widths (moderately DDR-future proof).
SPARCv2 on Bittware XUPVWH

- Check portability with Virtex Ultrascale+
- HBM2 Interface
- Low-latency PCIe
- Compatibility with a 10-100 GbE network

Projected capabilities
- HBM2 on the Xilinx Ultrascale+ VU-series chips can provide a theoretical peak bandwidth of 460 GB/s (4-6 boards for NFIRAOS MVM bandwidth)
- VU37P – 9,024 DSP48E2 (2-3 boards for NFIRAOS FLOPS)
THANK YOU

QUESTIONS?
