Avinash Surendran
IIA, Bangalore

IUCAA, Pune
(Prof. A. N. Ramaprakash)

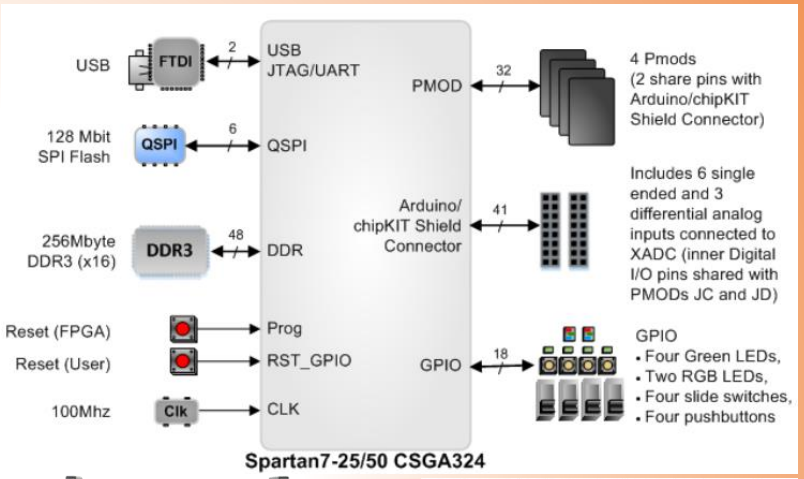
A Scalable Platform for Adaptive optics Real-time Control on FPGA

From small telescopes to ExAO

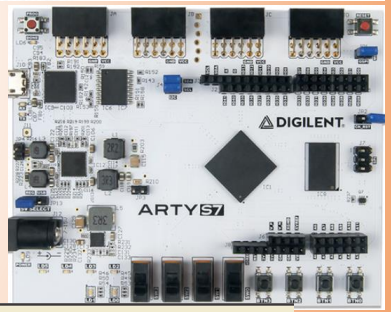
AO on small telescopes

- Plug-and-play AO (simple architecture) with off-the-shelf development boards.
- Compatibility with Arduino shields (standardization) with higher FLOPS/chip area compared to MCUs.
- Inexpensive and portable, with standard interfaces.

Courtesy: Digilent



Courtesy: Microgate



Extreme-AO

- Extremely low jitter and latency requirements.
- Large MVM and memory bandwidth.

	Status	DM[a]	Primary WFS(s)[b]
Palm3000+P1640, Palomar (5 m)	Operation 2012–2017	66	SHWFS, 2 kHz
GPI, Gemini (8.2 m)	Operation 2014–present	50	SHWFS, 1 kHz
SPHERE, VLT (8.2 m)	Operation 2014–present	50	SHWFS, 1.2 kHz
SCExAO, Subaru (8.3 m)	Operation + development	48	Pyramid, 3.6 kHz
MagAO-X, Magellan (6.5 m)	Development	48	Pyramid, 3.6 kHz

Courtesy: Guyon (2018)

Scalability

Targets

- Number of subapertures and pixels per subaperture
- Memory bandwidth (DDR-scalable, HBM/HMC in future).
- Interoperable with Xilinx FPGAs

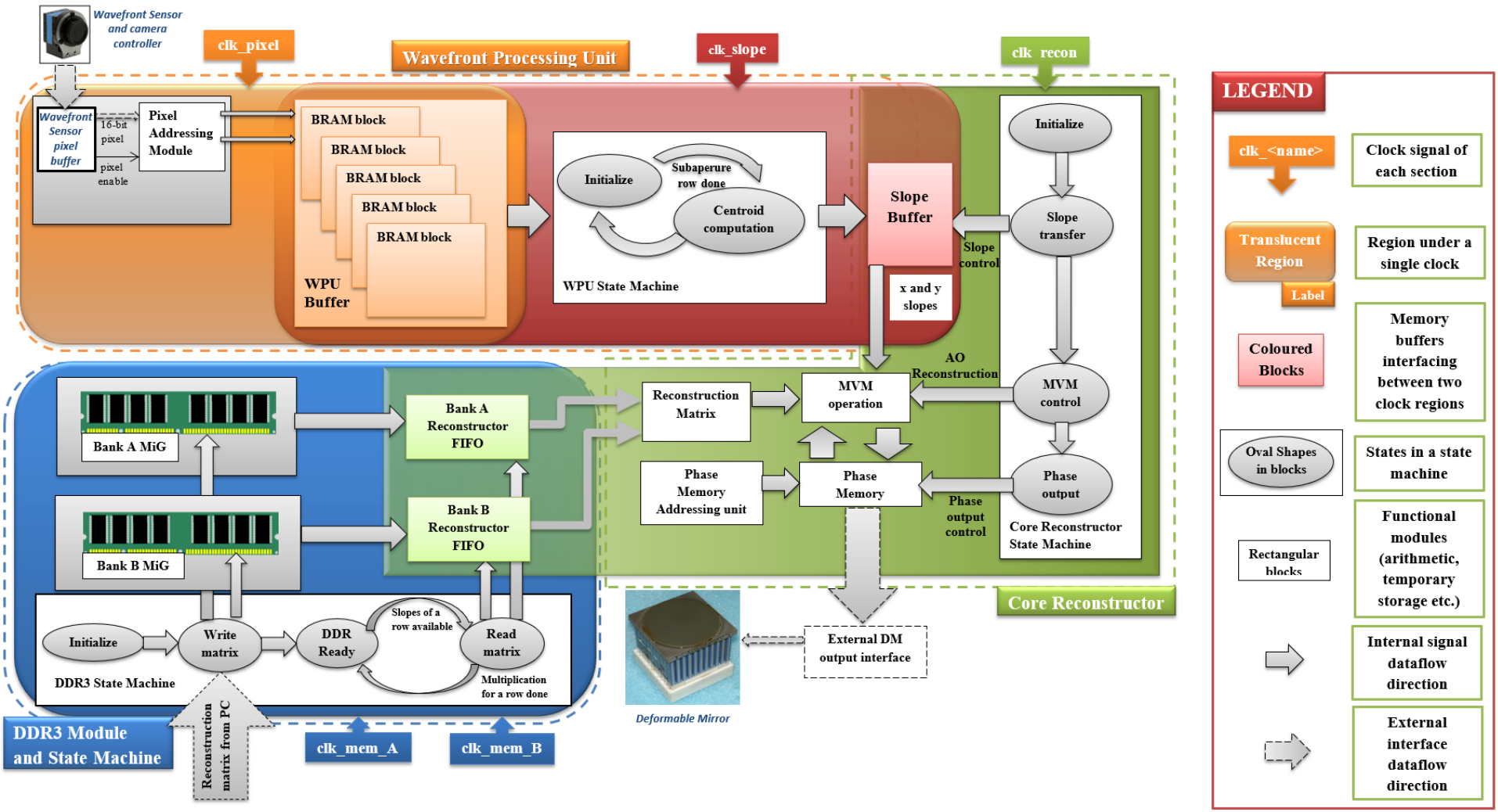
Challenges

- Programming Overhead
- Backward Compatibility

Implementation

- Xilinx VC-709 with Virtex-7 690T and 2x4GB DDR3 (12.8 GB/s peak per chip)
- Before HMC and HBM2

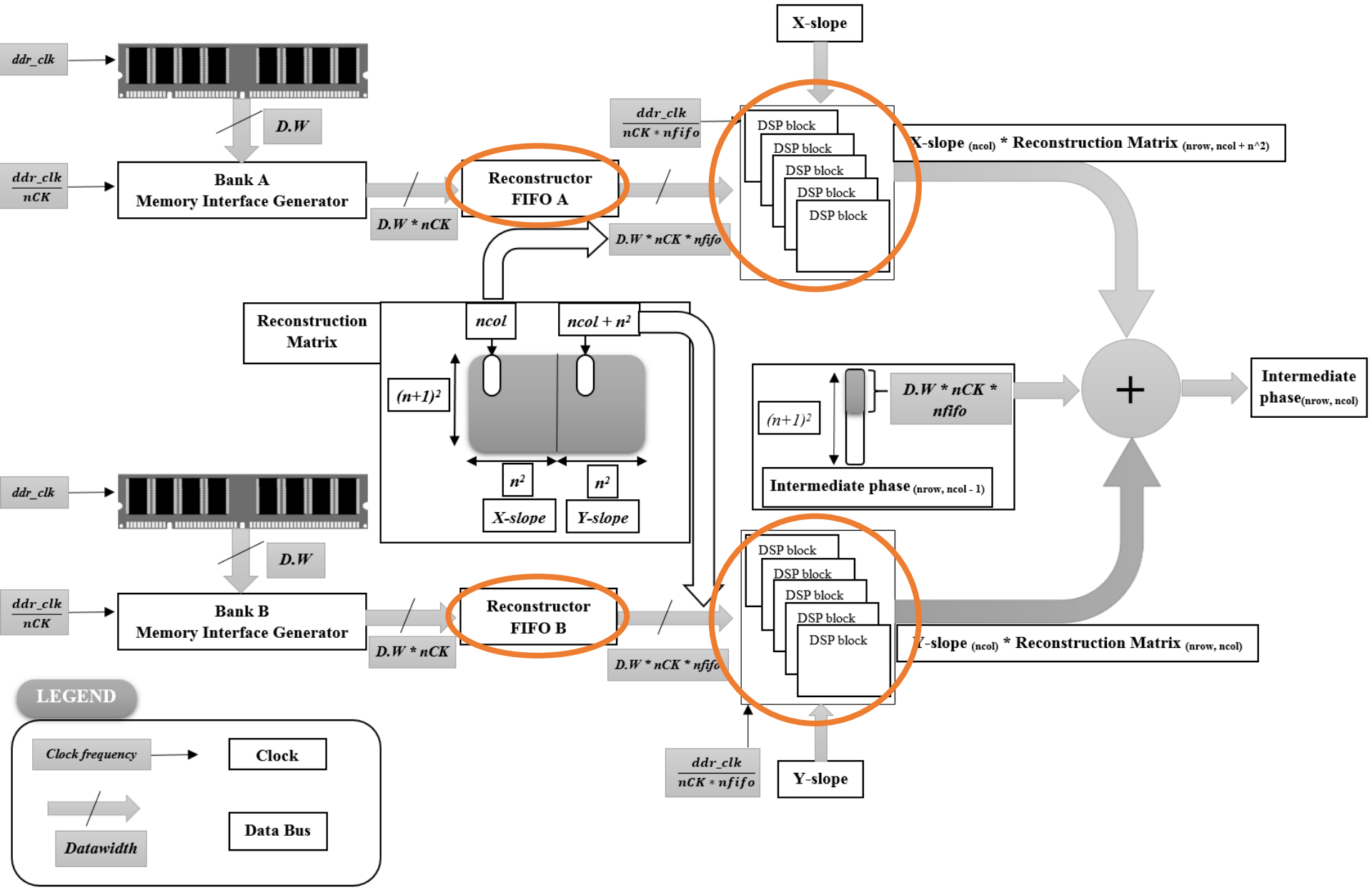
Dataflow


Wavefront Sensor and camera controller
clk_pixel
Wavefront Processing Unit
clk_slope
clk_recon
Wavefront Sensor pixel buffer
16-bit pixel
pixel enable
Pixel Addressing Module
BRAM block
BRAM block
BRAM block
BRAM block
BRAM block
WPU Buffer
Initialize
Subaperure row done
Centroid computation
WPU State Machine
Slope Buffer
x and y slopes
Slope control
Initialize
Slope transfer
MVM control
Phase output
Core Reconstructor State Machine
AO Reconstruction
Reconstruction Matrix
MVM operation
Phase Memory Addressing unit
Phase Memory
Phase output control
Bank A MiG
Bank B MiG
Bank A Reconstructor FIFO
Bank B Reconstructor FIFO
Core Reconstructor
Initialize
Write matrix
DDR Ready
Slopes of a row available
Read matrix
Multiplication for a row done
DDR3 State Machine
DDR3 Module and State Machine
Reconstruction matrix from PC
clk_mem_A
clk_mem_B
External DM output interface
Deformable Mirror
LEGEND
clk_<name>
Clock signal of each section
Translucent Region
Label
Region under a single clock
Coloured Blocks
Memory buffers interfacing between two clock regions
Oval Shapes in blocks
States in a state machine
Rectangular blocks
Functional modules (arithmetic, temporary storage etc.)
Internal signal dataflow direction
External interface dataflow direction

Dataflow

- **WPU –** Acquire pixels from CCD interface, and scalable slope computer (clk_pixel and clk_slope). Flexible BRAM addressing and modular slope computation.
- **AO Reconstructor –** Adapts to the memory speed (of the reconstruction matrix) and computes the DM outputs from WF slopes, by instantiating the required number of DSPs. Scalability of subapertures and memory speed implemented here.
- **Memory state machine –** Creates buffer between AO reconstructor and external memory. Intermediate FIFO can adapt to different datawidth and clock frequency of external memory

Scalability



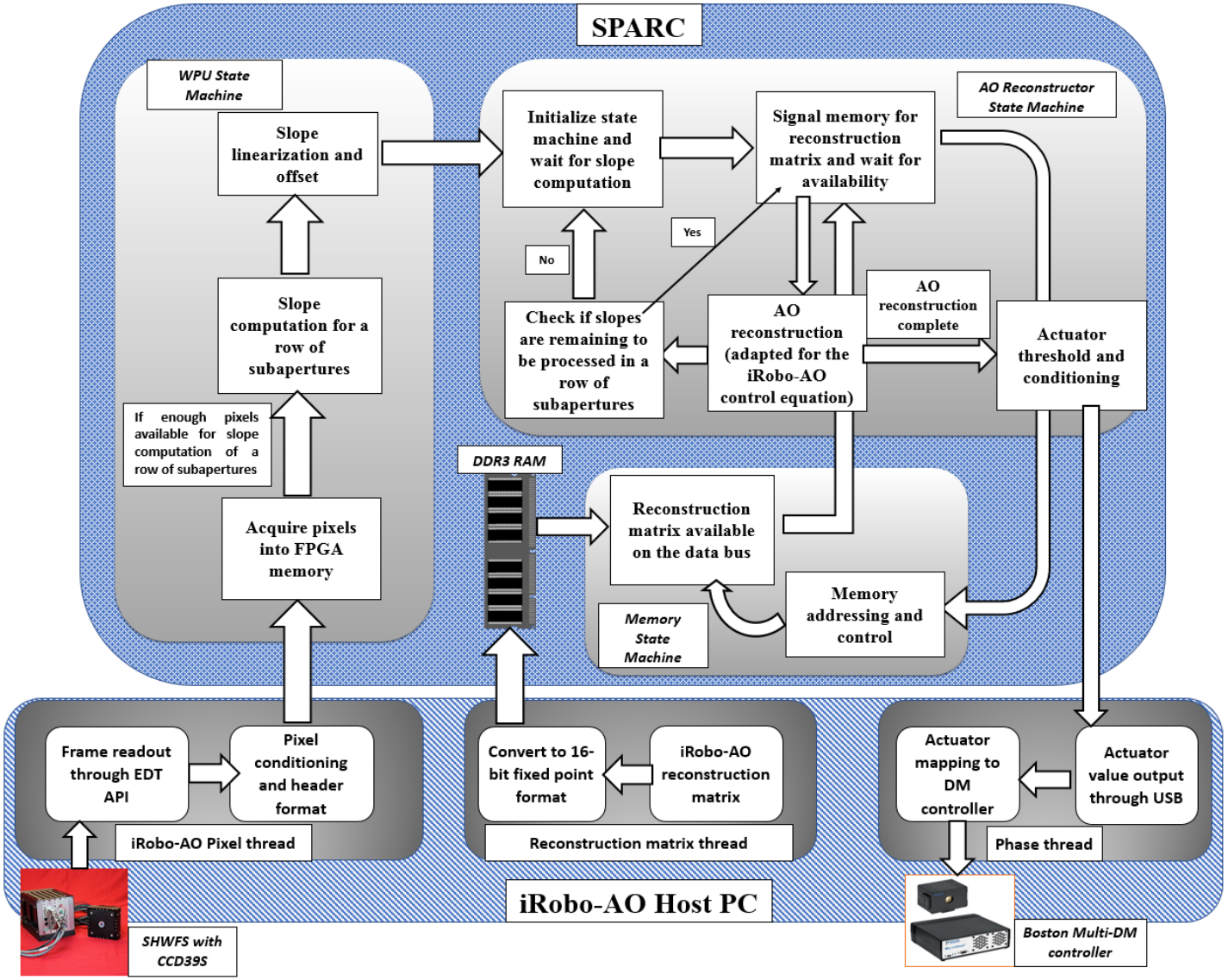
Scalability

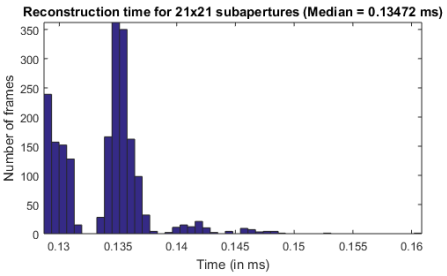
$$recon\_clk = \frac{ddr\_clk}{nCK \times nfifo}$$

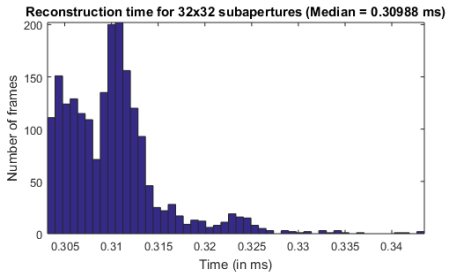
$$nfifo = \frac{ddr\_clk}{nCK \times recon\_clk}$$

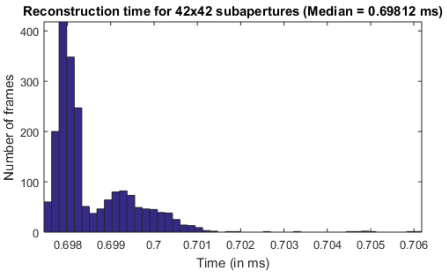
- **Scalability before synthesis, needs to be routed after scaling.**
- **512 DSPs per clock cycle for current DDR3. 3,600 DSPs available in 690T.**
- **Kernel determines RAM vs availability of DSPs and optimizes for maximum performance.**

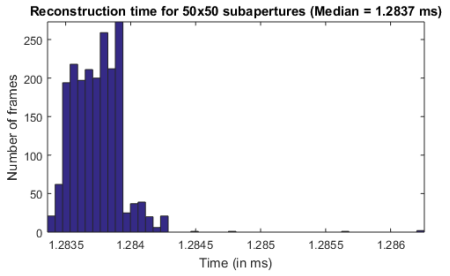
iRobo-AO

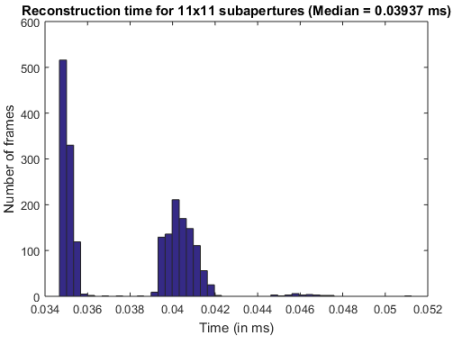

SPARC
WPU State Machine
Slope linearization and offset
Slope computation for a row of subapertures
If enough pixels available for slope computation of a row of subapertures
Acquire pixels into FPGA memory
Initialize state machine and wait for slope computation
Signal memory for reconstruction matrix and wait for availability
AO Reconstructor State Machine
No
Yes
Check if slopes are remaining to be processed in a row of subapertures
AO reconstruction (adapted for the iRobo-AO control equation)
AO reconstruction complete
Actuator threshold and conditioning
DDR3 RAM
Reconstruction matrix available on the data bus
Memory addressing and control
Memory State Machine
Frame readout through EDT API
Pixel conditioning and header format
iRobo-AO Pixel thread
Convert to 16-bit fixed point format
iRobo-AO reconstruction matrix
Reconstruction matrix thread
Actuator mapping to DM controller
Actuator value output through USB
Phase thread
iRobo-AO Host PC
SHWFS with CCD39S
Boston Multi-DM controller

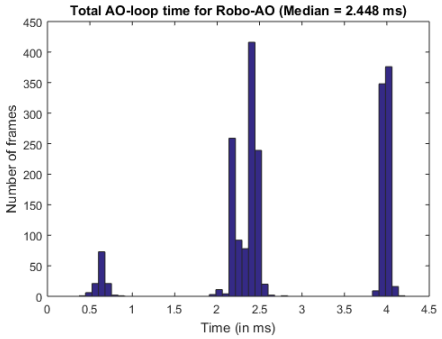










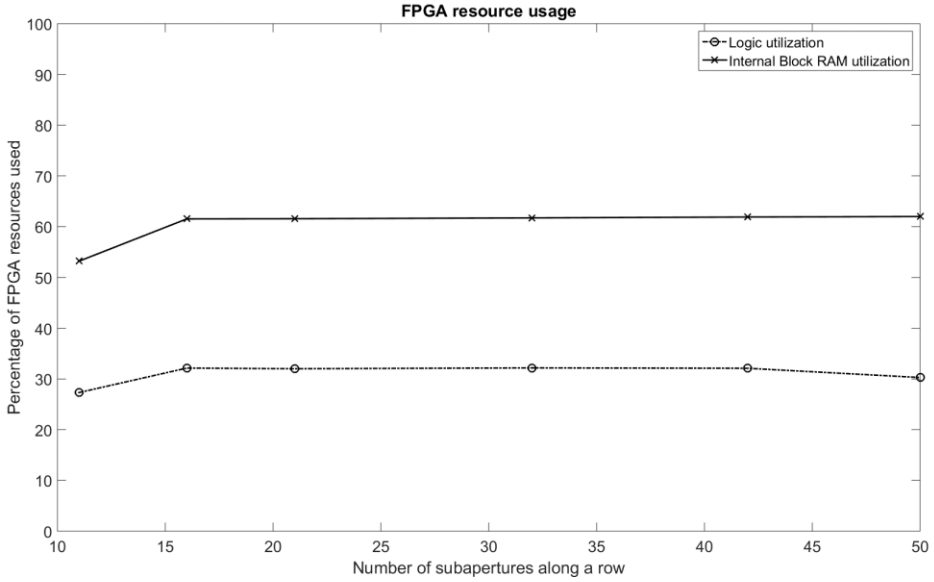


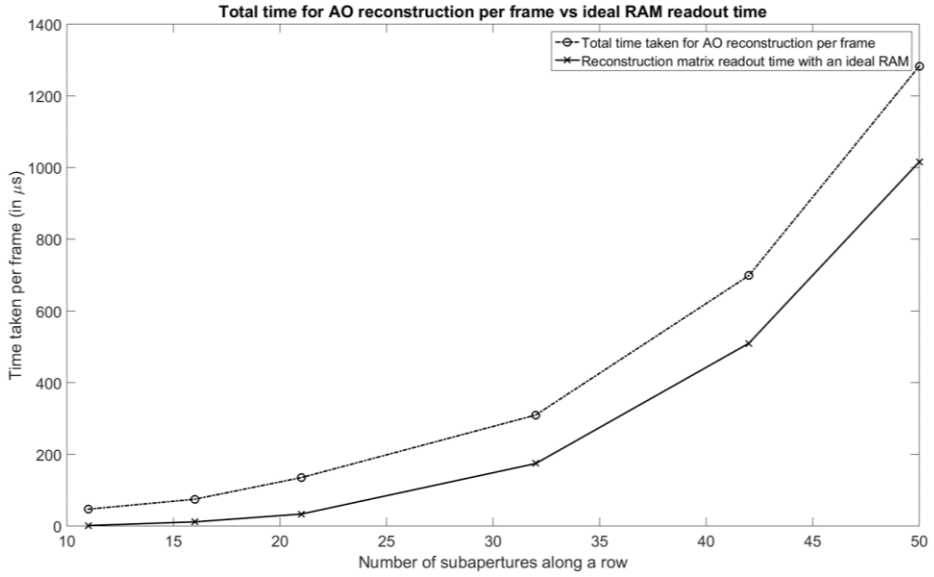
(a) (b)

Table 1 AO correction at different subaperture sizes and telescope aperture diameters. The input wavefront is simulated with a Fried parameter (r_0) of 15 cm, a mean wind velocity ($\overline{v}$) of 5 m/s and an outer scale of turbulence (L_0) of 25 m

Subapertures	Aperture Diameter (in meters)	Mean RMS WFE (in radians)			Strehl Ratio	Factor of Improvement in RMS WFE
		Input wavefront	Residual wavefront	Fitting + Time delay error		
50×50	8	9.03	0.54	0.62	0.75	16.77
42×42	6	5.10	0.43	0.57	0.83	12.07
32×32	5	3.44	0.33	0.60	0.90	10.63
21×21	4	2.18	0.24	0.70	0.94	9.25
16×16	3	1.49	0.27	0.68	0.93	5.64
11×11	2	0.99	0.20	0.65	0.96	4.92

HIL Simulation and iRobo-AO loop

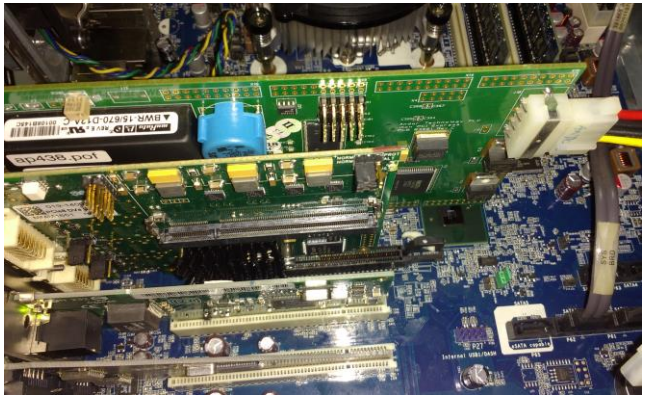




Resources, Memory and Time

Summary

- Median time of 1.283 ms from availability of first WFS pixel at the FPGA to the last actuator value exit at the PCIe interface.
- Real time AO reconstruction performance of 21.4 GFlops for an external memory bandwidth of 21.4 GB/s (16-bit fixed-point).
- FPGA resource usage of less than 30 %.
- FIFO buffer allows for the isolation of external memory enabling automatic adjustment of memory modules of different clock frequencies and data-widths (moderately DDR-future proof).

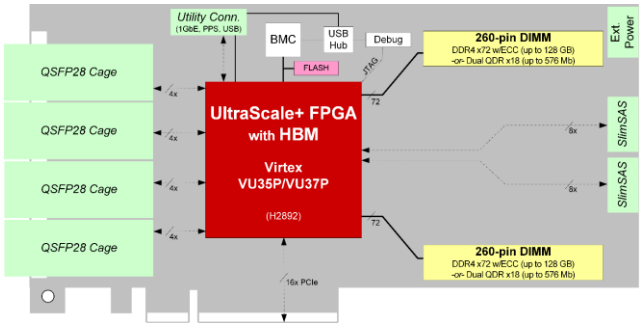


SPARCv2 on Bittware XUPVVH

- Check portability with Virtex Ultrascale+
- HBM2 Interface
- Low-latency PCIe
- Compatibility with a 10-100 GbE network

Projected capabilities

- HBM2 on the Xilinx Ultrascale+ VU-series chips can provide a theoretical peak bandwidth of 460 GB/s (4-6 boards for NFIRAOS MVM bandwidth)
- VU37P – 9,024 DSP48E2 (2-3 boards for NFIRAOS FLOPS)



Courtesy: Bittware

Device Name	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)	962	962	1,907	2,852
CLB Flip-Flops (K)	879	879	1,743	2,607
CLB LUTs (K)	440	440	872	1,304
Max. Dist. RAM (Mb)	12.5	12.5	24.6	36.7
Total Block RAM (Mb)	23.6	23.6	47.3	70.9
UltraRAM (Mb)	90.0	90.0	180.0	270.0
HBM DRAM (GB)	4	8	8	8
HBM AXI Interfaces	32	32	32	32
Clock Mgmt Tiles (CMTs)	4	4	8	12
DSP Slices	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)	8.9	8.9	18.6	28.1
PCIe® Gen3 x16 / Gen4 x8	4	4	5	6
CCIX Ports[1]	4	4	4	4
150G Interlaken	0	0	2	4
100G Ethernet w/ KR4 RS-FEC	2	2	5	8
Max. Single-Ended HP I/Os	208	208	416	624
GTY 32.75Gb/s Transceivers	32	32	64	96

Courtesy: Xilinx

THANK YOU

QUESTIONS?

- A. Surendran, M. P. Burse, A. N. Ramaprakash, *et al.*, "Scalable platform for adaptive optics real-time control, part 1: concept, architecture, and validation," *Journal of Astronomical Telescopes, Instruments, and Systems* 4, 4 – 4 – 11 (2018).
- A. Surendran, M. P. Burse, A. N. Ramaprakash, *et al.*, "Scalable platform for adaptive optics real-time control, part 2: field programmable gate array implementation and performance," *Journal of Astronomical Telescopes, Instruments, and Systems* 4, 4 – 4 – 8 (2018).